Design of a Low-Cost High Speed Data Capture Card for the Hubble Sphere Hydrogen Survey

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for the degree of Master of Science in Engineering.

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Declaration

I understand the meaing of plagiarism and declare that all work in the document, save for that which is properly acknowledged, is my own unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

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Cape Town

South Africa

November 11, 2008

Abstract

This thesis describes the design and implementation of a low-cost high speed data capture card for the Hubble Sphere Hydrogen Survey (HSHS).

The Hubble Space Hydrogen Survey was initiated in an effort to build a low-cost cylindrical radio telescope for an all sky redshift survey with the observational goal to produce a 3-dimensional mapping of the bulk Hubble Sphere using Hydrogen 21cm emissions[1].

This dissertation first investigates the system design to see how each of the user specifications set by the planning team in [33] could be achieved in terms of design decisions, component selection and schematic capture. The final design, *AstroGIG*, satisfies the user specifications by capturing data up to a full power bandwidth of 1.7GHz with an instantaneous bandwidth of $\leq$250MHz while maximizing the dynamic range. *AstroGIG* buffers, processes, stores and finally transmits the data through a 4-lane PCI-Express interface to a standard PC where the majority of the processing is performed. The system implementation is then described where issues relating to the process of transforming schematics into a physical PCB, and HSHS integration are discussed. The design is verified through *Hyperlynx* simulations to give a high degree of certainty that physical implementation and production would be successful. Results from tests on the actual hardware characterizing the overall system performance are presented. Conclusions are drawn based on these results and suggestions for future work and design improvements are recommended.

[1] $\approx$1420MHz Electro-Magnetic (EM) emissions due to spin/flip transfers

To my family,

for all their support

and guidance. If not for all of you,

I would not be the man I am today.

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Glossary

ADC — Analogue-to-Digital Converter

AFE — Analogue Front End. This is the named given to the group of components between the SMA and ADC data input pins.

BALUN — Balanced/Unbalanced Transformer. A device used to connect a circuit (unbalanced) one of whose two conductors is grounded to a two conductor circuit (balanced) neither of whose conductors is grounded and visa versa.

DDR — Double Data Rate

DLL — Delay Locked Loop

ECM — Extended Control Mode. This is the named given to ADC operation whereby eight 32-bit internal registers are updated using the 3-wire serial interface - similar to an SPI interface - in order to control several advanced features.

ENOB — Effective Number of Bits

FPBW — Full Power Bandwidth (Encode Bandwidth)

FPGA — Field Programmable Gate Array. They feature a programmable gate-array-like architecture with a matrix of logic cells surrounded by a periphery of I/O cells.

FR-4 — Flame Retardant 4. This is a type of material used for making a printed circuit board (PCB).

Harmonic Distortion — Overtones produced when a simple signal wave is sent through a circuit with nonlinear electrical characteristics. This is usually measure in *dBc*.

HSTL — High Speed Transistor Logic

JTAG — Joint Action Test Group. Interface for in-circuit debugging and testing.

LVDS — Low Voltage Differential Signal

Noise Figure — Noise figure of a receiver is a measure of how much the receiver degrades the ratio of signal to noise of the incoming signal. It is related to the minimum detectable signal.

RAM — Random Access Memory

SERDES — Serialize/De-serialize. Usually the name given to FPGA high speed transceivers.

SFDR — Spurious Free Dynamic Range.

SINAD — Signal to Noise and Distortion. The ratio of total signal to the sum of noise and harmonics.

SWR — Standing Wave Ratio. The measurement of the amount of RF energy reflected back into the transmitter by the antenna.

VCO — Voltage Controlled Oscillator

Chapter 1

Introduction

Many physical quantities in the universe are continuous-valued and can often be measured as analogue values by scientific instruments. There are many advantages to performing data processing using digital techniques, and this is the predominant method [67]. The bridge between analogue and digital subsystems is now the Analogue-to-Digital Converter (ADC). Ultra High-Speed ADCs have recently been released[1] with sampling rates of 3GSPS and Full Power Bandwidth (FPBW) extending up to 3GHz. The resolution of these ADCs are typically specified at 8-bits, giving rise to data rates of up to 3GB/s. Although computing speeds have increased, where inexpensive standard PCs can perform real-time Fast Fourier Transforms (FFT) with bandwidths of a few hundred Megahertz [33], specialized hardware is required to process data rates extending into the Giga-Hertz range. In the past, these hardware modules were application specific and could not be easily upgraded to accommodate for technological advances. According to Moore's Law, they would become obsolete before they were commissioned [1]. There has thus been a shift away from traditional computing to reconfigurable computing architectures. These reconfigurable modules, developed using dedicated Field Programmable Gate Arrays (FPGA), allow the adjustment of the data processing pipeline without the need to change hardware modules. FPGAs allow over 10 times the computing power of existing systems and are extensively implemented in applications requiring high data rates and digital signal processing [1]. A working application of modular reconfigurable architecture can be seen in the the Berkeley Emulation Engine (BEE2) system which is fully documented in [14, 1].

An application combining both high-end conversion and reconfigurable computing is proposed in the design of the data processing unit of the cylindrical array telescope for the Hubble Sphere Hydrogen Survey (HSHS). The objective of this dissertation is to describe the design, development and implementation of a high-speed data capture card for the

[1] See National Semiconductor website `www.national.com` \ Atmel website `www.atmel.com`

HSHS. Specifically, concepts relating to high speed digitization, the design process, implementation via firmware coding and finally testing through different testing strategies are discussed.

1.1 Background of Investigation

Modern understanding - through recent observations [73, 2] - reveals a universe that is expanding at an accelerating rate. This acceleration is thought to be attributed to the phenomenon of 'Dark Energy' or in other terms, a negative pressure acting as an anti-gravity agent. A wide variety of methods have been proposed to measure the expansion history. Measurement of baryon acoustic oscillations have shown the most promising results[2]. However, using this method *"only the brightest one percent of the of luminosity function need to be detected to reach the cosmic variance limit"* and thus an all sky redshift survey would constrain this expansion history [33].

According to Professor Jeffrey B. Peterson [33], in order *"to detect the 21 cm flux from high redshift galaxies, across the entire sky, in less than a year of observation, requires a collecting area of several hundred thousand square kilometers. Such a telescope would be about a factor ten larger than any in existence today."* It is therefore proposed that an all sky redshift survey be carried out whereby cylindrical reflectors could be used [33]. These would be constructed by suspending a flexible cable to a support at either end which under tension of gravity, would take on an almost parabolic shape. 'Back-side' stay cables could be added to keep the structure stable under varying wind conditions. Cylindrical reflectors became popular in the 1950's because of their large collecting area and low-cost design. The flaw in this design was the many expensive cryo-genically cooled low-noise amplifiers that were required for each node on the cylindrical array. The invention of HEMT low-noise amplifiers (LNA) and advances in RF and digital electronics have renewed interest in this reflector topology as a viable option in modern radio astronomy. An example of a fixed mesh cylindrical reflector can be seen in the Molonglo Observatory Synthesis Telescope (MOST) of *Figure 1.1* located near Canberra, Australia. The MOST is operated by the School of Physics of the University of Sydney and was constructed during the 1960's [3].

1.2 Project Scope

The Hubble Space Hydrogen Survey was initiated in an effort to build a low-cost radio telescope for such an all sky redshift survey. The observational goal is to produce a 3-

[2]Refer to `http://t8web.lanl.gov/people/heitmann/darkuniverse/bao.html` for more information

[3]Refer to MOST website `www.physics.usyd.edu.au/astrop/most/` for more information

Figure 1.1: The Molonglo Observatory Synthesis Telescope (MOST)

dimensional mapping of the bulk Hubble Sphere[4] using Hydrogen 21cm emissions. A prototype version of the HSHS, illustrated in *Figure 1.2,* is being constructed at Carnegie Mellon University, USA. The evenly spaced feeds from each node on the cylindrical reflector are summed with a small time delay as described in [33] and Digital Signal Processing (DSP) is performed on the output feeds.

In late 2006, one of the project drivers, Prof. Jeffrey B. Peterson (Carnegie Mellon University) approached the University of Cape Town (UCT) and the Karoo Array Telescope (KAT) to design data capture hardware, optimized for use in a standard PC environment. This hardware would form part of the analogue-to-digital conversion process required for data capture and processing (*Figure 1.2*). The scope of the proposal included the design and implementation from schematic level through to PCB design, layout and testing.

1.3 User Specification

The requirements are extracted from [33], defining the design specifications, functionality and any other constraints to which the final product must comply. These identified requirements were refined and finalized in further discussions with Prof. Peterson.

1.3.1 User requirements

The user requirements are:

- The Analogue-to-Digital Conversion process shall have an analogue bandwidth B_{range} of 500MHz to 1500MHz.

[4] A sphere centered on Earth with radius of about 7 billion light years

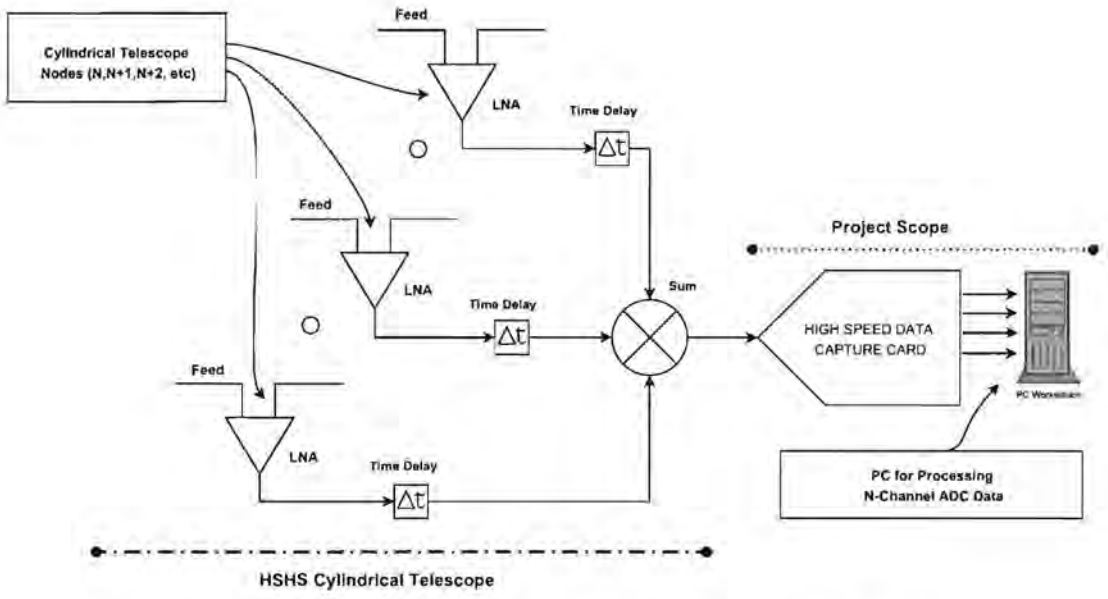


Figure 1.2: System Architecture of the Hubble Sphere Hydrogen Survey

- The instantaneous sampling bandwidth B_{inst} is set at 200MHz.
- Simultaneous sampling of two independent channels with $8bits$ sampling resolution per channel.
- The theoretical maximum analogue input signal is to be 1Vpp into 50Ω as per other industry standard digitizers such as the Acqiris digitizer range[5].
- On-board ADC sampling clock running at ≈500MHz - referenced to a frequency $f_{ref} = 10$MHz - for remote application.
- The digitizer card should be capable of accepting an external sampling clock and trigger. The trigger must be able to be synchronized with the system clock to ensure coherence.
- A FPGA must be chosen from the ECP2M device family from *Lattice Semiconductor* [43].
- Communications between the digitizer card and the host PC is to utilize a 4-lane PCI-Express architecture.
- Frequency resolution to be acquired by Digital Signal Processing (DSP) should be $f_{res} \leq 25$kHz which equates to $\approx 40\mu$s of sampling time per channel at a sampling rate of 500MSPS[6].

[5]See Acqiris website `www.acqiris.com`
[6]See Wikipedia `http://en.wikipedia.org/wiki/Short-time_Fourier_transform`

1.3.2 Functional Requirements

The following are the functions that the system must be capable of performing in order to satisfy the project scope of *Section 1.2*:

1. Capture the analogue signal with adequate bandwidth and resolution for the application.
2. Capture samples by latching the data into the FPGA where it can be buffered, manipulated and translated to/from other peripherals and interfaces. The FPGA is required to act as the master, applying control signals to all other peripherals.
3. Stream data across the PCI-Express link for continuous, 'real-time' DSP.
4. The FPGA must support on-the-fly reconfiguration through uploading a new boot image through the PCI-Express bus.
5. Act as a 'stand-alone' test-bench unit that does not require to be inserted into a PC. Programming is accomplished by uploading the synthesized *.bit configuration file[7] into the FPGA with the *Lattice ISPVM USB Cable*, allowing for either JTAG or SPI Flash programming. The later option provides the user with a non-volatile method of storing the FPGA configuration data.

1.4 Requirement Analysis

This analysis considers the above user specifications and translates them into pure electrical engineering terms, thus describing how each requirement can be achieved.

The analysis showed the user requirements to be very constraining with many of the hardware aspects already specified. Therefore, no investigation or cost/benefit analysis was conducted into other FPGA manufacturers (ie: *Xilinx* or *Altera*) nor standard PC interfaces (ie: PCI, USB or HTX). The design had to exhibit a clear separation between the analogue and digital modules to limit contamination and degradation of the sampled signal. The design topology of *Figure 1.3* was singled out as the most efficient and effective design strategy as it employs dedicated point-to-point interfaces eliminating the need for complex bussed networks[8]. This allows for each interface to be designed, optimized and debugged independently. Special attention is required for the high speed interfaces with respect to signal integrity, impedance and length matching.

The modules within *Figure 1.3* that were not specified in the user specifications and which are needed to adhere to the required functionality are:

[7] Created in the *Lattice Semiconductor ISPLever* toolkit

[8] Echoed in *Xilinx, National Semiconductor and Lattice Semiconductor* reference designs

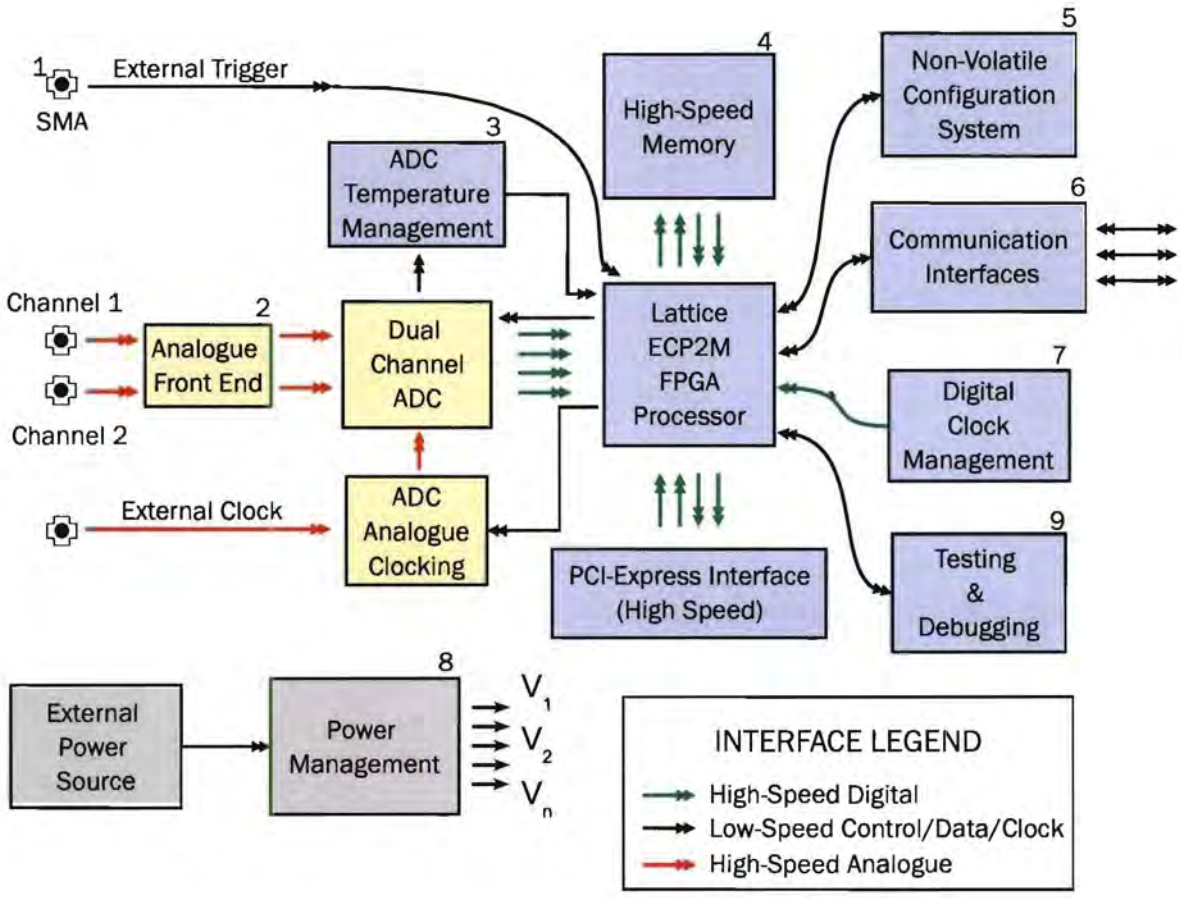


Figure 1.3: Top-Level Topology of the System Design

1. SMA Connectors mounted on the front side of the PCB to accept the analogue signal input signals, external trigger and clock.

2. An Analogue Front-End (AFE) is necessary to condition the input signal to meet the full scale input range of the ADC as well as matching the input impedance of the ADC, minimizing reflections.

3. Temperature Management allows the effects of temperature drift of the sampled signals to be accurately modelled. The FPGA can power-down the ADC if the devices enters thermal run-away.

4. High speed memory for data storage and buffering. The implementation of the external memory does not form part of the project scope but is included for future development of the 'data streaming' application.

5. As the FPGA has a volatile configuration space, non-volatile boot memory allows for 'stand-alone' operation.

6. Serial communications through RS232 and JTAG for system control and debugging. This also includes mounts for attaching daughter boards or a logic analyzer to the FPGA.

7. System clocks to switch/toggle the FPGA fabric with suitable timing constraints.

8. Power supplies with the correct output voltages and timing characteristics. The timing would be independently controlled with supervisor ICs.

9. Status/Debugging indicators such as test-points and LEDs

1.5 Dissertation Overview

The structure of this dissertation is as follows:

CHAPTER 2 describes the system design within the architecture of *Figure 1.3*. Special attention is directed to design issues resulting in design decisions, component selection and ultimately schematic capture. Various aspects of design and selection are validated through calculation and simulation. Project schematics are hierarchically captured in *Mentor Graphics DxDesigner*. This software package provides an easy-to-use, scalable design interface capable of integrating with multiple layout tools across a wide variety of computing platforms.

The chapter commences by outlining the principles of wide-band conversion, with a view to understanding the criteria for ADC specification, in terms of inception into the HSHS. Using these criteria, a survey of commercially available Off-The-Shelf (OTS) ADCs is

conducted where two potential dual 8-bit 500MSPS samplers are identified. These ADCs are compared with respect to their performance characteristics, resulting in the selection of the *National Semiconductor* ADC08D500. A functional description of this ADC is given, showing the design implementation. This ADC requires a full scale analog differential input of ≈750mVpp while in Extended Control Mode (ECM) and thus the problem of transforming the 1Vpp input signal is addressed. The implementation of BALUN transformers to convert from a single-ended to differential input signal is discussed with the limiting factors being that of power consumption, operating frequency and distortion. *Octave*[9] simulations of BALUN transmission line equations, predict the required input voltage of 1.5Vpp, allowing for the attenuator/gain system to be fully designed. Care is taken as not to reach the compression and 1st and 3rd intermodulation points of any of the selected components. A critical aspect of sampling performance, clock jitter, is then introduced. Jitter on the sampling clocks results in sampling voltage errors which degrade the overall system SNR. The maximum allowable clock jitter is calculated to be 2.44psRMS for a frequency up to the Nyquist rate. With this information, the design of the ≈500MHz frequency synthesizer - consisting of a PLL, Loop Filter and VCO - is discussed and simulated to validate conformation to the maximum jitter specification.

Attention is then diverted away from analogue to digital design, beginning with the high speed memory. Several high speed architectures are reviewed resulting in the selection of QDRII memory. Considerations in implementing this memory with the ECP2M FPGA are reviewed. The project scope does not require an in-depth understanding of the PCI-Express architecture because interconnect attributes, fabric management etc. would be addressed within the FPGA SERDES and OTS PC motherboard. Therefore, only an overview of the PCI-Express interface and Electro-Mechanical specifications considered in the design stages are presented. Debugging interfaces are briefly overviewed, but form an integral part of hardware verification. The design and operation of the ECP2M FPGA is fully described with reference to I/O planning, clock management, SERDES/PCS and non-volatile configuration. Finally, the design of the power management network in terms of power estimation, distribution and sequencing is discussed.

This then concludes both analogue and digital system design sections. The following is so far achieved:

- Issues encountered in translating the user requirements into pure electrical engineering terms are discussed.
- Design decisions are justified through through calculation and simulation.
- Components selected.

[9]High-level language, primarily intended for numerical computations that is mostly compatible with *MATLAB*

- System design is shown to have the capability of conforming to the user specification.
- Schematics fully captured in *DxDesigner*.

CHAPTER 3 focuses on the implementation phase of the project where issues are discussed relating to the process of transforming schematics into a physical PCB. For reference purposes every project requires a formal name and thus the digitizer was coined the *AstroGIG*. The chapter is divided into two subdivisions, covering PCB (including verification through post-route simulation) and software implementation:

- **PCB Implementation:** In an effort to support local business, only South African based companies are used in the production of the *AstroGIG* digitizer. Information extracted from their production specifications set the layering, routing and placement constraints to which the PCB could be implemented. Motivation is offered for manufacture with a particular card profile and FR-4 8-layer stack-up. Routing rules for characteristics such as impedance matching, differential pairs and length matching are formulated. These rules define the routing constraints for the autoroute process. With the stack-up chosen and rules defined, concerns about power planing of the multiple board voltage levels are brought forward. Component placement in order to minimize crosstalk and reflections in sensitive signals is justified. Visual/Oscilloscope simulations are performed on all critical nets using IBIS models[10]. Simulation models are investigated to explain the the non-monolithic behavior of certain waveforms about I/O trip points. A method for waveform rise-time compensation is found to rectify the problem. Visual simulations are time consuming because only a selective group - defined by a crosstalk voltage range - can be executed together. Batch simulations are implemented in order to simultaneously calculate the Signal Integrity (SI) performance of any amount of nets on the entire PCB in a single iteration. Timing margins for firmware design can be derived from these simulations. Finally, a costing analysis compares the final product with surveyed market equivalents to confirm a 'low-cost' design. Design CAM documentation (Gerber files) can be found in Appendix *F*.
- **Software Implementation:** The methodology in programming the FPGA in order to get it 'up and running' using the Lattice Software is listed. A summary of the modular firmware design for testing and integration into the HSHS is illustrated and explained.

At this point of the project the following can be concluded:

[10] – These include the interfaces between the FPGA and ADC, QDRII and PCI-Express.

- Decisions as to FR-4 stack-up, component placement, voltage planing distribution and routing constraints were seen to bare heavily on reducing crosstalk and increasing SI.
- *Hyperlynx* provides an invaluable tool in signal integrity analysis and gives a high degree of certainty that physical implementation and production would be successful.
- The high speed interfaces of the ADC, QDRII and PCI-Express are fully simulated and should perform as specified in their respective electrical specifications.
- The *AstroGIG* is capable of competing with OTS digitizer units with the same functionality in a cost sensitive environment.
- The finalized PCB is routed, simulated and ready for production.

CHAPTER 4 centres around the results of tests performed on the final system to validate categories of both hardware functionality and analogue performance. Functional tests serve to prove that the system does what is expected (conforms to the specification of *Section 1.3*) where as performance testing characterizes the analogue behavior. This testing strategy focuses on firstly validating individual interfaces and then secondly combining each module to fulfill the required functionality of the project scope. The obtained results are discussed and analyzed.

A range of general functional system tests are carried out to check factors such as power supply stability, JTAG/flash programming and external resets. The 3-wire serial interfaces (PLL and ADC) are then probed so see if the firmware correctly configures and calibrates the devices. Once these tests have been deemed successful, the functionality of the PCI-Express interface is assessed through the manipulation of the existing *PCI-Express Endpoint IP Core Demo for Lattice ECP2M and SCM*[44]. The original design - illustrated in *Figure 1.4*[11] - is intended for the *LatticeECP2M x4 PCI Express Evaluation Board* but is altered through changing the sample 'pin file' to match the designed schematics. This PCI-Express demonstration is defined to prove the functionality and capability of reading/writing data to the FPGA via the PCI-Express interface.

With the functionality testing completed, system performance is assessed. The AFE is shown to exhibit $\approx$ 3.45dB gain and perform the single-ended to differential conversion with the predicted behavior. The input port voltage reflection coefficient (s_{11}) for both ADC input channels is found for an input frequency range f_{in} where 4.5MHz$\leq$ f_{in} $\leq$2GHz. Frequency synthesizer operation and performance is evaluated with respect

[11] Adapted from *Figure 6* in [44]

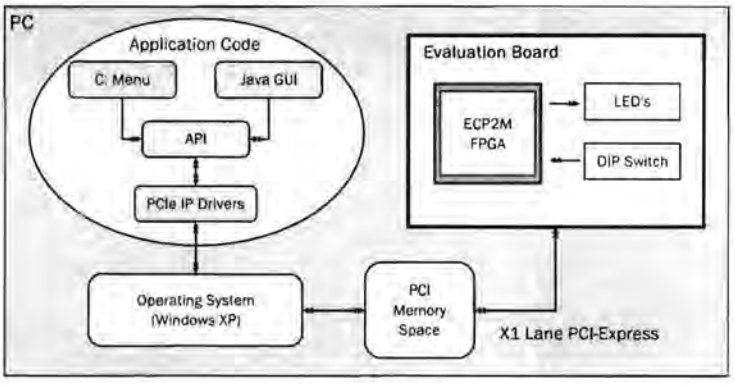


Figure 1.4: PCI-Express Demonstration HDL and Software

to voltage and power levels, jitter and tuned frequency. Oscilloscope waveforms are captured to show that these parameters meet the designed clock signal requirements with $\approx$ 1Vpp differential amplitude, $\approx$ 500MHz frequency and $\approx$ 1.86psRMS jitter.

Sampled datasets of various input signals of frequency 5MHz$\leq f_{in} \leq$1.4GHz are acquired by using an external clock source. These sampled datasets are transmitted to the PC via the RS232 interface where they are analyzed in *MATLAB* 7.0. The time domain data is plotted and a FFT is used to transform the data into the frequency domain where the SFDR can be determined.

The chapter concludes with an analysis of the testing results where conclusions surrounding issues relating to both of the above categories are presented and discussed.

CHAPTER 5 is where the conclusions that will be drawn up as to the success of the project are identified. Based on these conclusions, suggestions for future work and design improvements will be recommended.

Briefly the conclusions are:

- A hardware platform was developed that conformed to the user requirements for the HSHS. The design and implementation process included:
  - Transforming the user specifications into pure electrical engineering terms as well as understanding the principles and concepts involved in mixed signal design (analogue and digital signals).
  - Schematic capture, board layout/routing and simulation of routed PCB with the interpretation of the simulated results in making minor adjustments to the design.
  - FPGA firmware development in both VHDL and Verilog.

- A low cost design was achieved as the *AstroGIG* is approximately ZAR 8000 cheaper than an OTS unit with similar functionality. Coupled by the *AstroGIG* having four times better theoretical output data rate than these OTS units, it is thus approximately the same order of magnitude more cost effective to implement.
- The system showed that it was capable of functioning within the PCI-Express environment across multiple operating systems.
- The analogue performance of the system was found to be adequate for the signal processing applications of the HSHS. The noise floor was seen to be at $\approx$-65dB, with an average SFDR of $\approx$40dB for both input channels. The actual system SFDR could be higher as the frequency artifacts can be attributed to the coupling of FM radio signals (88MHz-108MHz), harmonics of the sampling signal aliasing back into the 1st Nyquist zone and the drifting of the both the signal and sampling clock sources.

Based on these conclusions, the following recommendations were made:

- Further the firmware to allow captured samples to be streamed across the x4 PCI-Express interface at an *optimized* rate.
- Develop an open-source driver that maps the sampled data to a pre-defined memory space for user operations without the need for proprietary software.
- Implement the QDR-II memory for data storage and buffering.
- Design improvements - listed in *Appendix E* - should be incorporated in subsequent versions of the *AstroGIG*.
- Extend the PCI-Express lane width to 8 lanes in order to increase theoretical output data rate of $\leq$2GB/s and negate any latency issues.

APPENDIX A - BALUN Simulation *Octave* Code

This appendix shows the open-source *Octave* source code for the simulation of the analogue front end.

APPENDIX B - FPGA Power Consumption Estimation

This appendix gives the tabulated results of the FPGA power estimation through *PowerCalc*.

APPENDIX C - *WebBench* Specifications

The parameters entered into the *WebBench* simulator from *National Semiconductor* used to test the performance of the frequency synthesizer is shown.

APPENDIX D - SPICE Loop Filter Simulation

This appendix presents the simulation comparison between *National Semiconductor Big Gig Reference Board* the and *AstroGIG* loop filter designs.

APPENDIX E - Design Errata

This appendix itemizes design errata that should be incorporated into subsequent versions of the *AstroGIG*.

APPENDIX F - DVD Attachment

A list of where to find source code, project files, documentation and simulations not included in the written thesis on the DVD attached to this thesis is given.

Chapter 2

System Design

This chapter discusses the design process of the HSHS digitizer and describes the system architecture under the constraints of the user specification. Reference schematics of the *LatticeECP2M™ PCI Express x4 Evaluation Board* [41] and *National Semiconductor Big Gig Reference Board* [28] were reviewed and served as design guidelines. Project schematics - presented in *Appendix F* - were captured in *Mentor Graphics DxDesigner* [51]. This software package provided an easy-to-use, scalable design interface capable of integrating with multiple layout tools across a wide variety of computing platforms. The Bill Of Materials (BOM) - given in Appendix F - was created in *Parts Lister*, a feature included in the *DxDesigner* package.

Finally, before the commencement of the chapter - it must be noted that only lead-free components were selected as to comply with the restriction of the use of certain hazardous substances in electrical and electronic equipment or ROHS directive[1].

2.1 Wide-band A-D Converter

There are two core principles to wide-band digitization namely, sampling rate and dynamic range.

Nyquist's Sampling Criterion places a restriction on the sampling rate f_s such that $f_s > 2B$ where B is the signal bandwidth. As described in [17], the bandpass sampling theory places yet further limitations on the minimum sampling rate so that the pass-band does not cross the $\frac{Nf_s}{2}$ boundary. These conditions have to be adhered to in order to preclude aliasing and unambiguously represent the captured band-limited signal in discrete samples. It is therefore implied, that an instantaneous bandwidth of $\approx$ 200MHz would require $f_s \geq$ 400MHz.

[1] Refer to ROHS website `http://www.rohs.gov.uk/content.aspx?id=9` for more information.

Dynamic Range (DR), mathematically defined as $DR_l = \frac{Ps_m}{Ps_{min}}$ where Ps_m and Ps_{min} is the maximum allowable signal power and minimum detectable signal power respectively[2], is the measure of the system's ability to accurately distinguish a weak signal in the presence of noise and/or larger signals [17, 24]. Considered a valuable performance indicator, dynamic range characterizes the entire system within its operating environment, taking into account factors such as inherent ADC properties (i.e.: Linearity, ENOB), system noise and sampling jitter.

The above requirements needed to be optimized in the selection of an appropriate ADC for the HSHS.

2.1.1 ADC Comparison and Selection

A survey of commercially available, off-the-shelf (OTS) ADCs, identified two potential candidates, both in dual configuration, 8-bit resolution and 500 *MSPS* sampling rate. These were the ADC08D500 [59] and AT08AD004B [6] from manufacturers *National Semiconductor* and *Atmel* respectively. An advantage of these components is that devices within the same families of both manufacturers are pin compatible and thus the design can be easily modified to accommodate for a higher order ADC[3].

A careful performance comparison was performed as individual manufacturers may specify their component characteristics differently [17]. An example of this is if whether the dynamic converter characteristics are defined relative to full scale (dBFS) or relative to the carrier (dBc). Attention should also be drawn to the analogue input frequencies and power levels of the performed characterizing tests in the respective component's data-sheets, as certain characteristics such as ENOB degrade at higher frequencies. The identical comparison parameters and methodology implemented in [17][4] is applied to compare these A-D Converters. An explanation for each parameter can be found in [63, 8, 45].

A review of the comparison listed in *Table 2.1* - between typical electrical values in normal operational mode[5] - displayed the following conclusions:

- The AT08AD004B offers 4dB better two-tone intermodulation.
- The ADC08D500 exhibits a superior SNR, DNL and SINAD
- Both ADCs can be operated in extended control mode (ECM).

[2]Estimated using Friss link formula *[24]*

[3]i.e.: Higher sampling rate, bit width, analogue bandwidth etc.

[4]Refer to pages 34-36

[5]Non - 'Dual Edge Sampling (DES)' and 'Non-Interleave' modes in *National Semiconductor* and *Atmel* components respectively

- The AT08AD004B falls short of the full power input bandwidth range specified in the user specification.

As a result of this short review, it can be seen that the ADC08D500 exhibits superior performance characteristics within the context of this project and is therefore selected as the A-D Converter for the HSHS digitizer card.

PARAMETER	NATIONAL ADC08D500[a]	ATMEL AT08AD004B[b]
Maximum Sampling Rate (MSPS)	500	500
Number of bits	8	8
Full Power Bandwidth (GHz)	1.7	1
SNR (dBFS)	47.5	45
SINAD (dB)	47	43
Aperture Jitter (ps RMS)	0.4	0.4
Worst Harmonic Distortion (2nd or 3rd) (dBc)	-65	-53
Total Harmonic Distortion (dBc)	-55	-53
Two-tone IM Distortion (dBc)	-50[c]	-54[d]
Differential non-linearity (LSBs)	0.2[e]	0.25[f]
Integral non-linearity (LSBs)	0.4[g]	0.4[h]
Extended Control	YES	YES

[a] Test conditions : Input frequency $f_{in} = 248MHz$, Sampling clock $f_{clk} = 500MHz$ and Input voltage $V_{in} = FSR - 0.5dB$

[b] Test conditions : Input frequency $f_{in} = 250MHz$, Sampling clock $f_{clk} = 500MHz$ and Input voltage $V_{in} = -1dBFS$

[c] Measured with input frequency: $f_{in1} = 121MHz$ and $f_{in2} = 126MHz$ with an input voltage $V_{in} = FSR - 7dB$

[d] Measured with input frequency: $f_{in1} = 249MHz$ and $f_{in2} = 251MHz$ with an input voltage $V_{in} = -1dBFS$

[e] DC Coupled, 1MHz Sine Wave Overanged

[f] $f_{in} = 1MHz$, $f_{clk} = 50MHz$ and Saturated Input

[g] DC Coupled, 1MHz Sine Wave Overanged

[h] $f_{in} = 1MHz$, $f_{clk} = 50MHz$ and Saturated Input

Table 2.1: Comparison Between the ADC08D500 and AT08AD004B ADCs

2.1.2 ADC08D500 Implementation

The analogue sampling module requires certain peripheral elements in order to fulfill the system functional requirements. An overview of the designed implementation - illustrated in *Figure 2.1* - is described:

A single linear voltage regulator, capable of supplying 1.9V@1.4W, drives both the analogue and digital sections of the ADC08D500. The power to these sections is however isolated through a ferrite bead.

The ADC is operated in Extended Control Mode (ECM), whereby eight 32-bit internal registers are updated using the 3-wire serial interface (*DATA,SCLK,CS*) - similar to an

SPI interface - in order to control several advanced features listed in [59]. Operational modes of power down and reset can be invoked by pulling certain physical pins on the ADC either high or low.

The analogue front end translates the 1Vpp input, for both I and Q channels, into the required driven full-scale A.C. coupled differential input signal of ≈750mVpp. This is approximately in the centre of the input voltage range of $560mV_{pp} \leq V_{in} \leq 840mV_{pp}$, while in ECM. Data is on acquired on the falling edge of $CLK+$ with the equivalent quantized data becoming available on the N-bit Low Voltage Differential Signal (LVDS) digital output buses approximately 14 clock cycles later. External termination resistors of 100Ω are needed to properly terminate the LVDS signals as the FPGA does have digitally controlled on-die termination found on Lattice *SC* devices. The design selects *DCLK* to operate in Double Data Rate (DDR) mode where digital output data is updated on both transitions of *DCLK*. This clock is specified at half the data rate which in turn is multiplexed to be half the rate of the input clock ($CLK+$and $CLK-$), bringing it into the realm of the ECP2M I/O and logic fabric. *DCLK* therefore synchronously outputs data at 125MHz for an input clock of 500MHz. An out-of-range signal (*OR*) is toggled whenever the input signal is clipped above/below the full scale range.

Calibration is performed through pulling the *CAL* pin low for 80 input clock cycles and then pulling it high for another 80 input clocks cycles. ADC calibration is performed on power-up or invoked by the user at any time during sampling. The calibration process trims the internal termination resistor and minimizes full scale error, offset error, DNL and INL which consequently maximizes dynamic range [72]. Calibration is indicated via the *CALRUN* signal.

Remote temperature sensing is required to monitor the on-die temperature diode in order for the user to model the effects of temperature drift and/or detect whether the component is operating in the specified temperature range.

An external trigger is passed through a Schmidt trigger comparator and traced directly into the FPGA, allowing synchronization of multiple digitizer cards in a networked environment.

The design of the analogue front end and clock circuitry modules are fully discussed in *Sections 2.2* and *2.3* respectively.

2.2 Analogue Front End

The receiver system, consisting of the interface between the SMA connectors and the ADC input, is often considered the most critical design component, as the integrity of

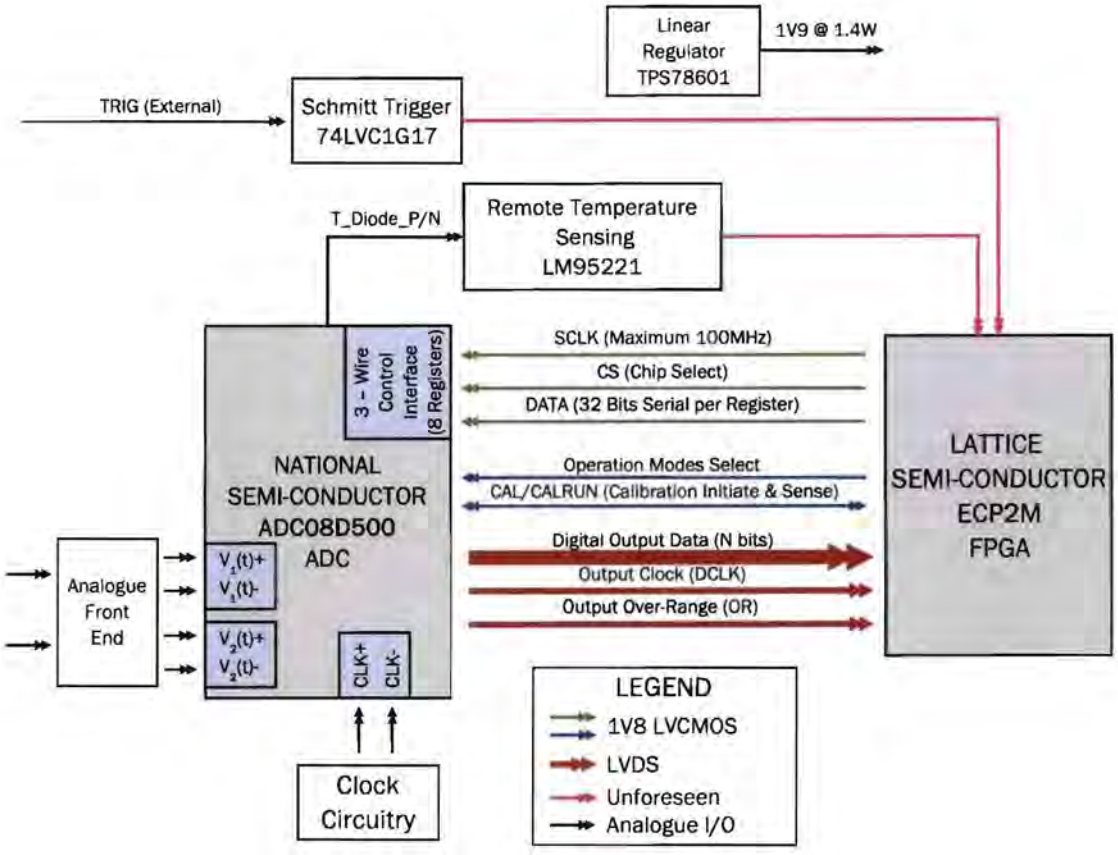


Figure 2.1: Interface Between the ADC08D500 and Other Peripherals

the sampled data is dependent on the reliability of the analogue circuitry to minimize the effects of reflections, noise and out-of-band interference [24].

According to [59], the ADC requires a full scale 750mVpp analogue input signal matched to 100Ω differential impedance. The design of the analogue front end was required to:

1. Convert the single-ended (*unbalanced 50Ω*) antenna feed to the required differential (*balanced 100Ω*) system at the ADC input while minimizing reflections.
2. Transform the specified maximum full-scale 1Vpp input signal [6] to the required 750mVpp.

An investigation was conducted into the methods of single-ended to differential conversion, resulting in two main implementation techniques of either using a *BAL*anced to *UN*balanced (BALUN) transformer or a fully differential amplifier such as the *National Semiconductor* LMH6555 [61]. The constraints in selection were power consumption and distortion in the conversion process. As per the tabulated comparison in [61], BALUNs offer lower power consumption, operating frequency range, and distortion whereas the LMH6555 has higher SNR and dynamic range. In application differences, the LMH6555

[6] Refer to Section 1.3

also requires an extra biasing circuit as a reference voltage. The decision was therefore taken to design with BALUN transformers following the guidelines mentioned in [61].

2.2.1 Balun Transformers

In general, BALUN or Transmission Line Transformers (TLT) are often used in matching networks for antennas in the HF and VHF range. These transformers frequently consist of a twisted pair or coaxial cable usually wrapped around a magnetic core to improve both low and high frequency limits. BALUNs operate by transmitting energy as a Transverse Electric and Magnetic (TEM) wave where the windings try to eliminate common mode currents. Each wire within the twisted pair carries equal currents but phase shifted by 180 degrees as in a differential transmission line [15]. As described in [16], a BALUN comprising of m transmission lines is classified as order-m. BALUN order has a direct consequence on the voltage transformation ratios, shown in [16]. In general, by obeying the rule that the ratio[7] of power in (P_{in}) vs. power out (P_{out}) must remain constant, the impedance ratio and thus the voltage ratio can be varied depending the winding topology. In general, if a BALUN exhibits an impedance ratio Ω of $1 : r$ then the current ratio and voltage ratio are $\sqrt{r} : 1$ and $1 : \sqrt{r}$ respectively.

In order to understand the impedance matching characteristics of TLTs, *Octave* was used to simulate the operation of a $1 : r$ BALUN within the ADC system of *Figure 2.2*. The synthesis equations (*Equations 2.1 and 2.2*) found in [16], are directly derived from standard transmission line theory presented in [24]. The system was excited by $V_{source} = A\sin(2\pi ft)$ where $A = 0.75$V[8]and f =1GHz. Various loads - with a set impedance ratio - were investigated to find which value of Z_{TERM} resulted in a load VSWR = 1. In simulation, Z_{in} was set to be equal to Z_{source} so that no reflections from the source to the input of the BALUN occurred. The characteristic impedance Z_0 of the BALUN was also calculated. Values of R_{in} and C_{in}were taken from [59].

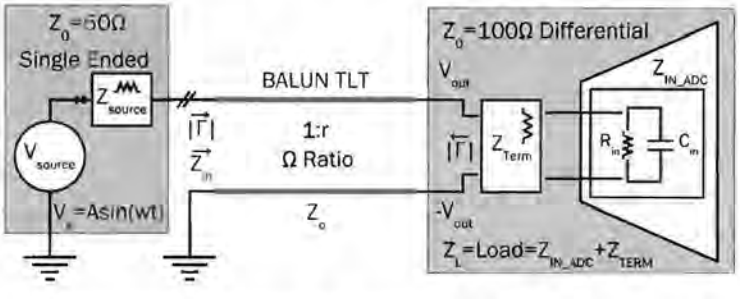


Figure 2.2: Balun Implementation for Single Ended to Differential Conversion

[7]Defined as the Output variable : Input variable

[8]The source amplitude value was chosen because of the implementation found in *Figure 18* of [61]

$$Z_{in} = Z_0 \left(\frac{R_L - Z_0 \tanh(\gamma l)}{Z_0 - R_L \tanh(\gamma l)} \right) \tag{2.1}$$

$$V_{out} = \frac{R_L}{2} \left(\frac{V_{in}}{R_L \cosh(\gamma l) - Z_0 \sinh(\gamma l)} \right) \tag{2.2}$$

The results of simulation (*Figure 2.3*) showed that for a 1:1Ω (*Figure 2.3b*) a 100Ω termination resistor was required to achieve the desired differential load voltage of 750mVpp with VSWR = 1 and $Z_0 = 50\Omega$. However, using a 1:2Ω BALUN (*Figure 2.3c*) without a termination resistor results in the equivalent reflection matching as the first case but with $V_{out} = V_{source} * \sqrt{r}$. This voltage would exceed the full scale ECM limit of the ADC analogue inputs. The use of the 1:1Ω BALUN minimizes reflections but has the disadvantage of only transmitting 3dB of the power to the load as power loss occurs over the transmission line. It was also seen that the ADC differential input capacitance only limits the upper frequency range and can thus be ignored [5]. The source code for the simulation can be found in *Appendix A*.

The *Mini-Circuits* TC1-1-13M+ 1:1Ω BALUN was selected as it provided excellent phase and amplitude unbalance with good return loss over the frequency range 4.5MHz$< f <$3GHz [54]. This component and its implementation is also recommended by both [61] and the SKA/KAT ROACH designs.

2.2.2 Attenuator/Gain Design

According to the experiments of Section 2.2.1, the ADC differential input of 750mVpp into 100Ω would transform into 1.5Vpp into 50Ω at the BALUN input. The analogue front end was designed by tracing the power levels of each module to match the 1Vpp to the required 1.5Vpp with an attenuator - gain topology illustrated in *Figure 2.4*. A 10dB attenuator was placed before the gain block to reduce the return loss of any mismatch between the antenna and the SMA input. All the components were selected from *MiniCircuits* with their respective part numbers marked in blue. Care was taken as not to reach their compression and 1st and 3rd intermodulation points, the methodology of which is described in [24].

2.3 ADC Analogue Clocking

The sampling process described in [17, 55], can be mathematically expressed as a convolution between the input signal and sampling clock. This is equivalent to a multiplication

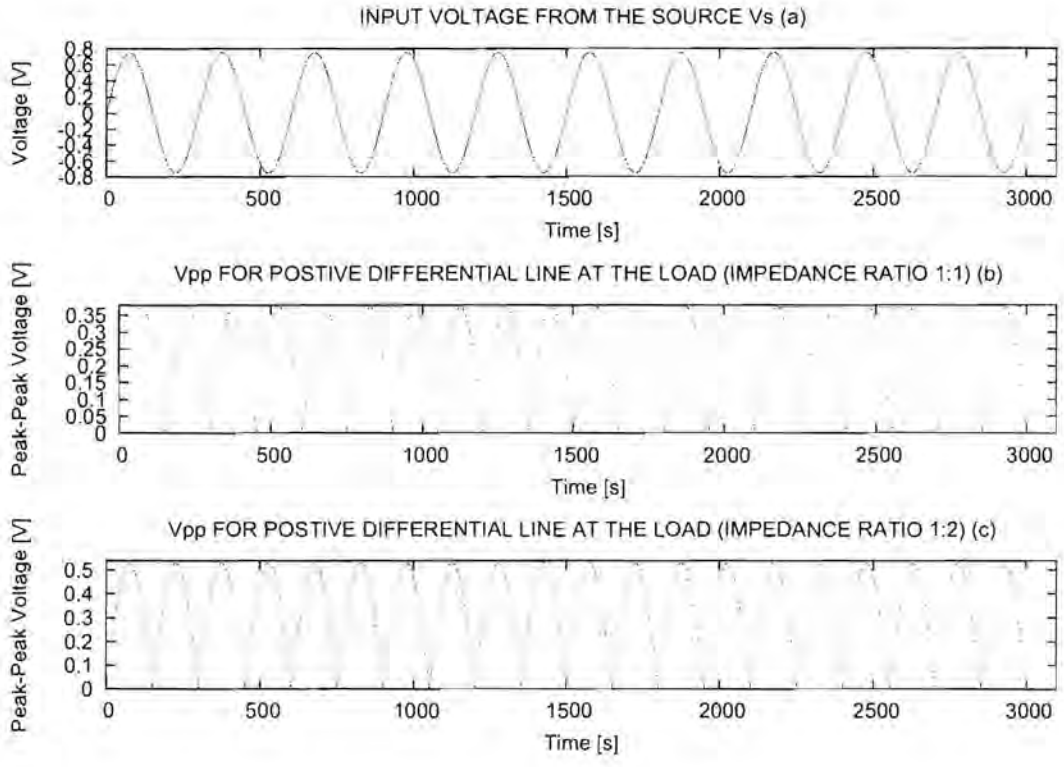


Figure 2.3: 1:1Ω and 1:2Ω BALUN Transformer Simulation

of spectra when translated into the frequency domain [9]. In theory, the sampling clock is considered as a train of Dirac deltas, equally spaced in time by the sampling period T_s (translated to spacing of ω_s in the frequency domain) [10]. However, in practice, the clock has inherent random time variations (jitter)[9]. These variations result in sampling voltage errors illustrated in *Figure 2.5*, which consequently degrade the overall system SNR.

Controlling the effects of clock jitter have always been an issue in analogue design but as clock speeds reach the GHz range, these factors become critical to the performance of these systems [62]. The design was required to implement a clocking circuit where the magnitude of the allowable clock jitter could be predicted and shown not to have adverse effects on the dynamic sampling performance.

2.3.1 Calculating the Maximum Allowable Clock Jitter

There are two main types of time jitter, namely quantifiable jitter, whose sources are identifiable (deterministic), and random jitter which follows a Gaussian distribution allowing for statistical analysis to be implemented [62] . The total contribution from all random jitter sources is found by taking the root mean sum of the squares of their individual sources and is expressed as:

[9]Measured as the time difference between the actual and ideal cycle period [22]

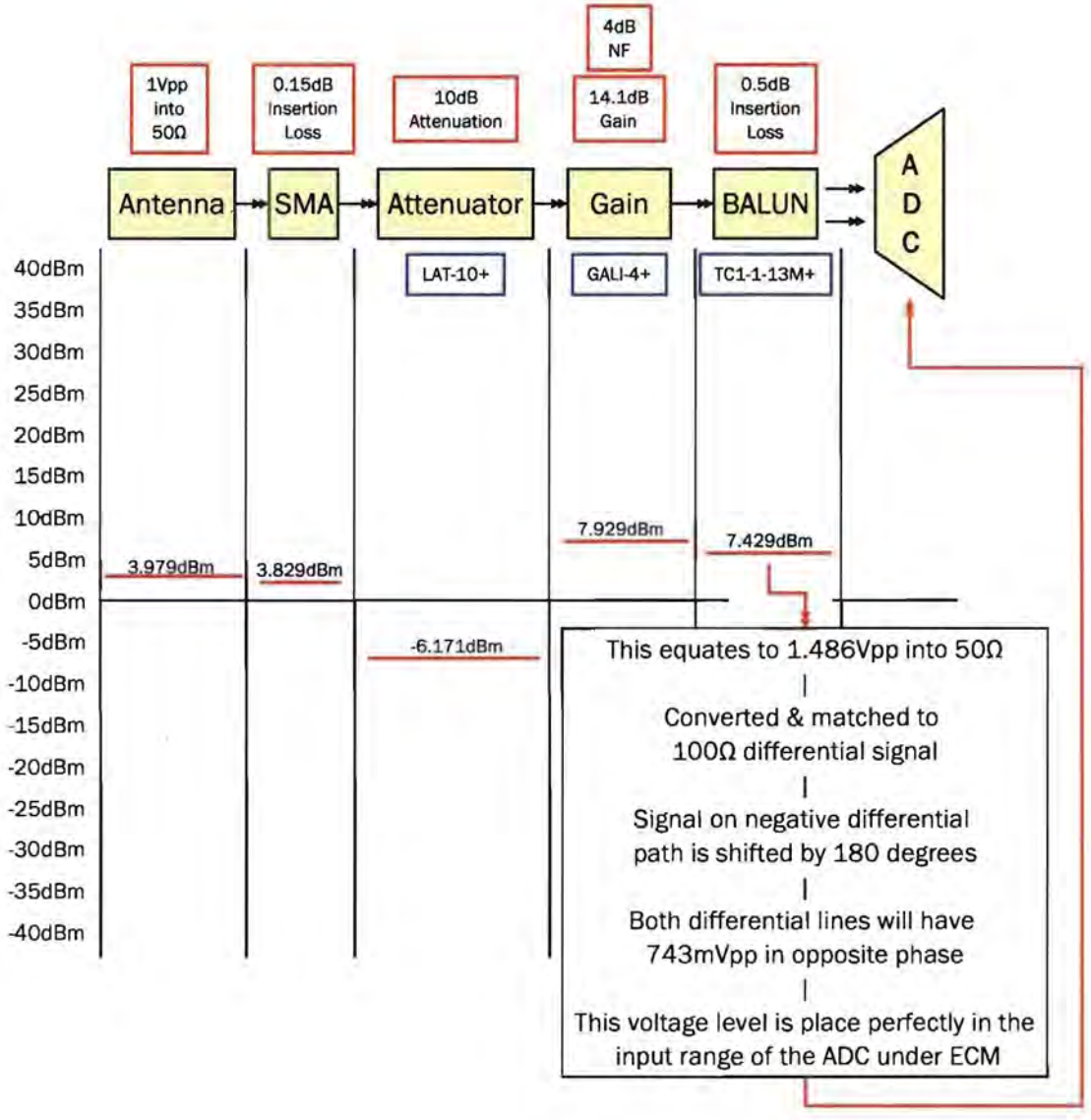


Figure 2.4: Design of the Analogue Attenuator/Gain Front End

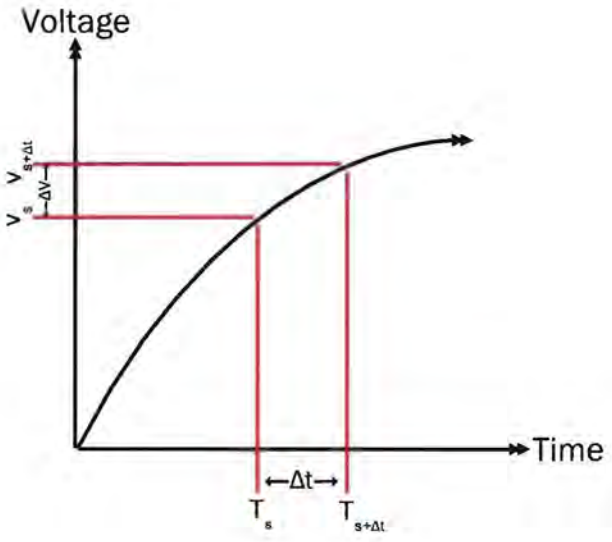


Figure 2.5: Sampling Voltage Errors Resulting From Clock Jitter

$$\sigma_t = \sqrt{(\sigma_{clk})^2 + (\sigma_{ap})^2}\ [ps\,RMS] \tag{2.3}$$

where σ_{clk} is the encode clock jitter and σ_{ap} is the A-D Converter aperture uncertainty. The complete A-D input SNR due to total jitter can thus be represented as:

$$SNR_j = 20\log\left(\frac{1}{2\pi f_a \sigma_t}\right)\ [dB] \tag{2.4}$$

where f_a is the analogue input frequency. The SNR_j is seen to deteriorate at higher input frequencies which is verified through inspection of the dynamic performance plots of [59] and by the fact the sampling voltage error increases with frequency (*See Figure 2.5*) [68]. In order to calculate the output SNR due to the entire system, the ADC quantization noise must be factored into *Equation 2.4*, resulting in:

$$SNR_t = 10\log\left(\frac{1}{\frac{1}{10^{\frac{SNR_j}{10}}} + \frac{1}{10^{\frac{SNR_q}{10}}}}\right)\ [dB] \tag{2.5}$$

Through simultaneous analysis of *Equations 2.4, 2.3 and 2.5* the maximum allowable clock jitter is calculated to be:

$$\sigma_{clk} = \sqrt{\frac{1}{(2\pi f_a)^2 * 10^{\frac{SNR_t}{10}}} - \sigma 2_{ap}}\ [ps\,RMS] \tag{2.6}$$

As a rule-of-thumb derived in Stremler [77], quantization noise $SNR_q = -(6.03N + 1.76)$ dBc where N is the ADC resolution in bits. The aperture uncertainty of the ADC08D500 is specified as 0.4ps and thus for a full scale input sinusoid of $f_a = 250$MHz and a recommended SNR_t of 46dB [29], the maximum allowable clock jitter - so that the jitter does not increase beyond $\frac{1}{2}LSB$ - is calculated to be 2.44psRMS. Jitter can further be minimized through the steps listed in [62].

2.3.2 Phase Noise

If an ideal sampling clock was used, the carrier power spectrum would appear as an infinitesimally thin line but due to time jitter[10], the oscillators power spreads into adjacent

[10]Through the Fourier Transforms inter-relationship between time domain delays and frequency domain phase modulation

frequencies [62]. In computation, it is easier to consider this power spreading in terms of the phase noise spectrum, derived by taking the ratio of the power in a 1Hz bandwidth at an offset frequency to the total power of the carrier [62]. Phase noise and clock jitter are therefore two different ways to look at the same phenomenon [68].

The main categories of phase noise are close-in and wide-band phase noise. The former, distorts the input analogue signal into other frequency components whereas the latter contributes to the degradation of the noise floor and can introduce reciprocal mixing [9]. Wide-band phase noise carries the relationship of periodically and repeatedly distorting the sampled spectrum into spur components around the sampling rate [62, 10]. If the encode bandwidth[11] is large relative to the sampling clock spectrum and the sampling clock phase noise extends beyond the 1st Nyquist zone, the effects of this noise will repeatedly alias back to base-band, through the Nyquist operation explained in [46], thus further degrading the SNR and dynamic range [10]. In the case of the ADC08D500, with an encode bandwidth of 1.7GHz and sampling frequency of 500MHz, the phase noise would alias approximately 7 times [9]. It is therefore imperative to consider the effects of clock phase noise on the sampling system.

2.3.3 Clock Circuit Design

A frequency synthesizer based architecture provides a cost effective solution for high speed clock generation as various clock frequencies can be obtained with a single configuration and reference oscillator [13]. The circuit presented in [29] - sharing the configuration of *Figure 2.6* - is recommended for design implementation. Part numbers of the components are marked in red. The programming of the internal registers is accomplished in exactly the same way as with the 3-wire serial interface described in Section 2.1.2.

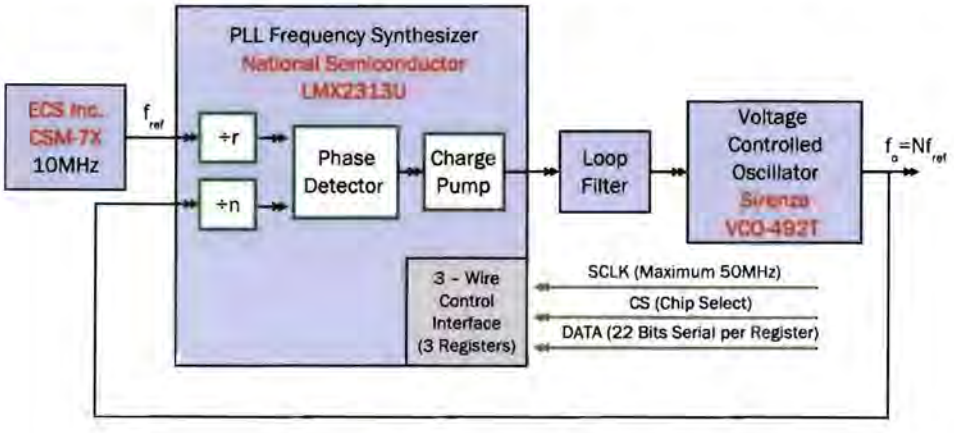


Figure 2.6: Frequency Synthesizer Design

The synthesizer (*Figure 2.6*) operates as follows:

[11] Equivalent to the FPBW

1. If the phase detector detects an error between the reference and output frequency (matched in scaling), current pulses are sourced/sunk into the loop filter (i.e. if $f_o \neq Nf_{ref}$). The length of these current pulses is proportional to the error.

2. The DC component of the current waveform is integrated and extracted by the loop filter and used as a smooth VCO tuning voltage which in turn outputs the desired frequency.

3. The VCO output frequency is fed back through an N divider where it is again compared to a scaled frequency of the reference oscillator until the loop-filter output voltage is stable.

Attention was directed to optimizing the key performance issues of phase noise, reference spurs and loop filter lock-time [3]. The trade-off lies between the transient response and noise feed-through of the filter which is approximated by $t = \frac{1}{B}$, where t and B are the lock-time in seconds and loop bandwidth[12] in Hertz respectively. In general, a narrow pass-band will reject the reference source input jitter but will not be able to counter any fast variations in the output frequency. Conversely, with a large loop bandwidth, VCO timing errors can be quickly corrected but at the expense of allowing more jitter through the system which can affect reciprocal mixing. In the first case the system is VCO noise limited where as in the second it is input jitter limited [13].

Optimization of the above effects requires the filter to be designed with a phase margin of $\frac{\pi}{4}$ [48] and a loop bandwidth $\leq \frac{1}{5}th$ of the phase detector channel spacing, for stability reasons [3]. Channel spacing refers to the minimum frequency resolution of the phase detector. In order to minimize output jitter and decrease lock time, the highest feasible channel spacing should be used. The easiest way to alter the loop bandwidth is by increase/decreasing the charge pump strength [3]. Calculating the values for the dividers can be found in the LMX2313U data-sheet [57].

2.3.4 Frequency Synthesizer Performance Analysis

The *WebBench* simulator from *National Semiconductor* was used to test the performance of the system[13] with the criteria given in *Appendix C*. The design was optimized for spur gain and channel spacing of 1MHz.

The simulated filter response (*Figure 2.7*) exhibits a closed loop bandwidth of 33.45kHz and phase margin of 47.18 degrees.

Each phase noise contributor, such as the loop filter resistors (R2 and R3) and the PLL crystal oscillator (TCXO), are independently shown in *Figure 2.8*. The total phase noise

[12] Defined as the $3dB$ cutoff

[13] See WebBench Simulator `http://webench.national.com/appinfo/webench/EasyPLL`

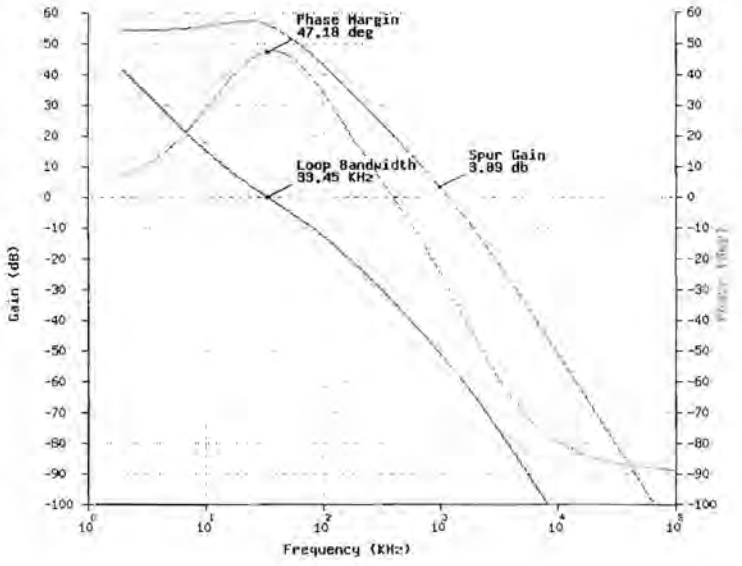


Figure 2.7: Gain and Phase Response of the Frequency Synthesizer Loop Filter

spectrum is shown as a solid black line. In order to calculate the system time jitter value, the resulting phase noise spectrum must be integrated over the full power bandwidth. Although this can be performed using logarithmic algebra described in [22], *WebBench* automatically calculates the RMS jitter value of σ_{clk}, which is 1.866psRMS. The synthesizer thus maintains the $SNR_t = 46$dB up to the Nyquist input frequency[14]. According to *Equation 2.6*, the maximum allowable f_a - before SNR_t is sacrificed below its recommended value - is calculated to be ≈420MHz. Sampling with $f_a = 1.5$GHz the SNR_t is calculated to be as low as ≈35dBc. The system also has an equivalent spur power of -47.641dBc.

In conclusion, these simulations show that the analogue clock circuit conforms to the specified parameters of jitter and SFDR and should not degrade the ENOB and hence the overall system SNR for $f_a \leq 420$MHz .

2.4 High-Speed Memory

A major concern for the future development of the digitizer was the uncertainty surrounding the bottlenecks and challenges faced in the streaming of data across the PCI-Express interface. The ADC05D500 maximum output data rate of 1GB/s is exactly equivalent to that of a 4-lane PCI-Express add-in card and therefore latency and throughput become issues. Although data channelization - through the implementation of DSP techniques on

[14]Refer to Section 2.3.1

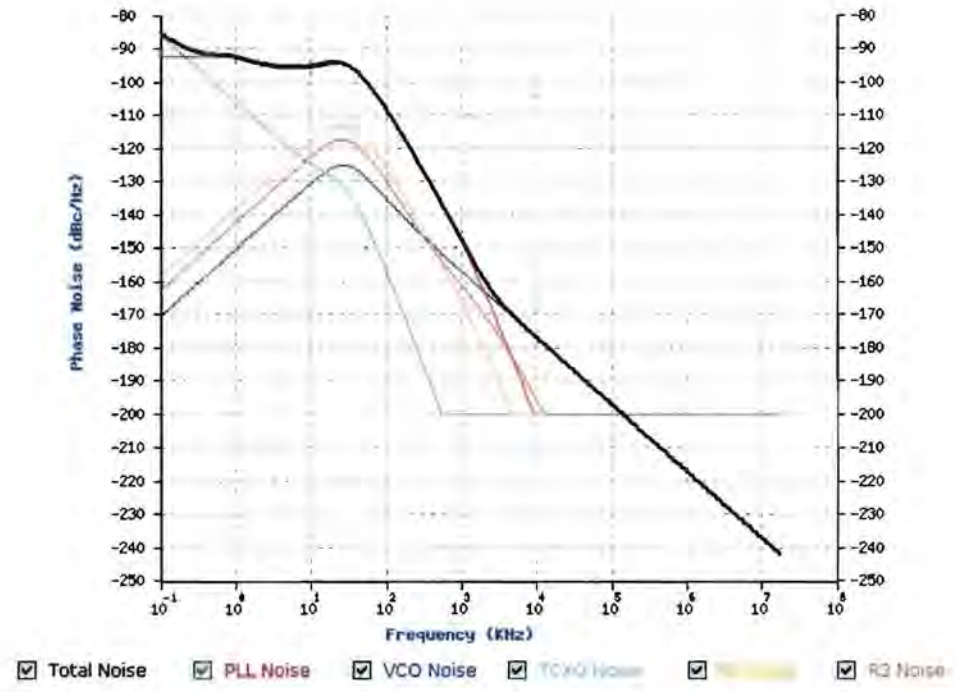


Figure 2.8: Phase Noise Spectrum of the Frequency Synthesizer

the FPGA - would reduce the channel bandwidth and allow for specific channels to be streamed to the host PC, data would still have to be captured, stored and buffered in an external memory.

2.4.1 Memory Selection

Demand for high performance systems in communications and DSP allows the evolution of memory device to closely match these requirements. Memory developers are trying to tackle issues of implementation, bandwidth, density, latency, power and cost with their next-generation memories. Unfortunately, a specific memory technology cannot simultaneously deliver solutions to all these problems and therefore memories are suited to specific applications [4]. The HSHS digitizer required a high bandwidth, low latency memory architecture.

According to the memory selection overview of [4], the second generation Quad-Data-Rate (QDRII) SRAM offered the most suitable solution because of its optimization for buffering/cache applications with a unity read/write ratio as well as providing a maximum channel bandwidth of 32Gb/s with densities of up to 72Mb. QDR is a synchronous pipelined burst SRAM with separate read/write buses whose technology is regulated through the QDR Consortium[15]. Issues of simultaneous switching noise (SSN) such as under/over-shoot and ground bounce - encountered by the earlier QDR generation -

[15]Refer to `www.qdrsram.com` for more information

are addressed in QDRII through on-die calibration. QDRII also offers only 5ns latency compared with 45ns of DDR2 as there is no bus turnaround time because of independent read/write ports. Latency is further enhanced through SRAM not requiring refresh cycles as is the case with its DRAM counterparts. The main disadvantage of the QDR family is that both power consumption ($mW/Mbit$) and cost ($cents/Mbit$) are approximately 40 times greater than DDR and DDR2. These factors however, only become important in a mass production environment and not in the prototype stages.

2.4.2 QDRII Considerations

The following considerations - with respect to the design implementation of *Figure 2.9* - were taken into account while designing with the *Samsung* K7R321882C QDR-II. Full functional descriptions and electrical characteristics can be found in [74, 20].

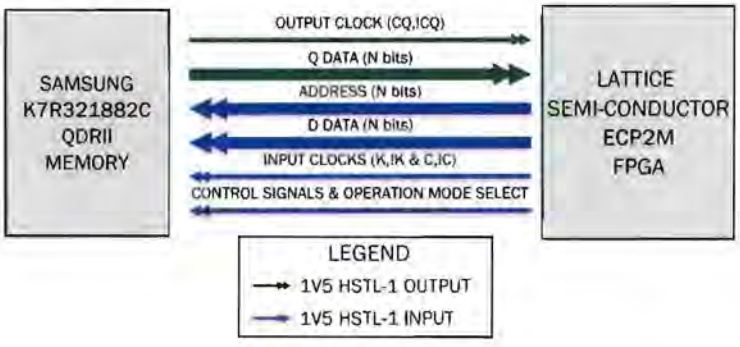


Figure 2.9: Interface Between the *Samsung* K7R321882C QDRII and ECP2M

2.4.2.1 Controller Module

There is no defined QDRII memory controller for the ECP2M device. Lattice Engineers were consulted on this matter and their response was:

"The ECP2/M devices should be capable of supporting the QDR-II devices from Samsung but Lattice has not tested the QDR-II interface in the ECP2/M devices."

Design was thus carried out in conjunction with the fully tested Lattice *ECP* reference design [39].

2.4.2.2 Clocking

Normally, QDRII input data and address lines are synchronized and transferred on every rising edge of $K or !K$ and transferred to the slave on every rising edge of $CQ or !CQ$ or

$C or !C$. If $C or !C$ - being the input clock for output data - are tied high then data outputs are synchronized to the input clocks $K or !K$. The latter option was not be chosen as it requires complex routing requirements and creates strict timing specifications relating to the flight time delay of the echoed clock [19]. BW operations for the 2 burst word device are supported [74]. According to [19], clock signals are not to be routed as differential pairs.

2.4.2.3 Initialization and Impedance Control

Initialization can either be performed pin controlled or clock controlled with the $\overline{Doff}$ pin. Clock controlled was implemented and therefore $\overline{Doff}$ was fixed high. A 250Ω 1% resistor - connected between the ZQ pin and Vss - set the output buffer impedance to $\frac{1}{5}$ of its value or in other words, matched the output impedance to 50Ω.

2.4.2.4 Power Management

QDRII employs the HSTL-1 standard for data transmission. This standard requires both a stable reference voltage and termination voltage of $\frac{VDDQ}{2}$ [26]. The termination voltage regulator must be capable of fast transient response in sourcing/sinking current. It is also recommended that supply voltages be planed rather than routed individually to each supply pin [20]. This must also be combined with the power sequencing requirement of VDD coming up before VDDQ [74].

2.4.2.5 JTAG

The JTAG interface of the QDRII was permanently disabled.

2.5 PCI-Express

PCI-Express was introduced by Intel in 2004 to replace the general-purpose Peripheral Component Interconnect (PCI) expansion bus, the high-end PCI-X bus and the AGP graphics card interface. The most significant difference between PCI-Express and previous architectures was the change-over from a shared bus topology, to a point-to-point full duplex serial 'link' for expansion interfaces. In PCI-Express terminology, a 'link' consists of two unidirectional LVDS pairs, while a 'lane' is used to group these pairs under a single entity. Each 'link' has a theoretical throughput of 2.5Gb/s in each direction

(before accounting for overhead)[16] and therefore the 4-lane digitizer card can theoretically transceive at 1GB/s in each direction[17].

The project scope did not require an in-depth understanding of the PCI-Express architecture - described in the PCI-Express Base Specification v1.1 [70] - because interconnect attributes, fabric management etc. would be addressed within the FPGA SERDES FPGA and OTS PC motherboard. This section is intended to serve as an overview of only those signals and specifications taken into account during schematic design.

2.5.1 Auxiliary Signals and Presence Detect

These signals are provided to assist with certain system level functionality or implementation but are not required by the PCI-Express architecture. Their electrical and timing characteristics can be found in [71]. Auxiliary signals were routed onto I/O pins of the FPGA except for the JTAG interface which was permanently disabled.

2.5.1.1 REFCLK

The 100MHz±300PPM LVDS reference clock was routed from the connector on the system board for use as the data synchronization clock on the add-in card. The REFCLK clock distribution timing budget allows for approximately 5mils trace widths with a maximum add-in card trace length of 4inches [71].

2.5.1.2 PERST#

The *PRSNT#* signal is used to indicate when the power supplies are within their specified voltage ,tolerance and are stable. This signal was connected in such a way that its assertion re-programs the FPGA.

2.5.1.3 SMBus

The optional I2C System Management Bus (SMBus) is a two-wire interface whereby system components can communicate to each other. SMBus provides a control bus for system and power management related tasks and is described in System Management Bus (SMBus) Specification, Version 2.0 [75]. The interface was connected to the FPGA, but its usage is not in the scope of this project.

[16] $8b/10b$ encoding is implemented in order to encode an embedded clock and to equalize the overall number of binary signal changes

[17] An informative, more detailed description of PCI-Express can be sought at: `http://arstechnica.com/articles/paedia/hardware/pcie.ars`, `http://www.interfacebus.com/Design_Connector_PCI_Express.html`, `http://en.wikipedia.org/wiki/PCI_Express`

2.5.1.4 Presence Detect PRSNT#

A PCI-Express card is required to fit into a slot[18] of its size or bigger, but not vice-versa. The digitizer board has a physical PCI-Express x4 connector, electrically wired to four FPGA SERDES transceivers. It therefore has the potential to operate in $\times 1$ or $\times 4$ PCI-Express slot [42]. The *PRSNT#* signal jumper selects the operating mode, by telling the protocol the number of active lanes to support.

2.5.2 Power Specifications

The following of power specifications affected the design of the digitizer power management system discussed in *Section 2.8*:

2.5.2.1 Consumption

Consumption is limited to 25W for a 4-lane PCI-Express add-in card and thus a careful estimation must be performed to aviod exceeding this limitation. The power rails can deliver the values listed in *Table 4-1* of [71].

2.5.2.2 Sequencing

There are no specific power sequencing requirements for the PCI-Express interface. The system controller, however, will assert the *PRSNT#* signal whenever any of the three power rails go outside of the specifications provided in *Table 4-1* of [71]. Power sequencing on the actual add-in card is the responsibility of the designer [71].

2.5.2.3 Power Decoupling and AC Coupling

Low level signaling - such as that implemented in PCI-Express signals - require sufficient decoupling to ensure noise does not create destructive interference in the data recovery of another upstream PCI-Express device. The guidelines itemized in *Section 4.4* of [71] were followed as closely as the design framework would allow.

The add-in card incorporates the necessary 100nF AC coupling capacitors on the transmitter differential pair required by [71].

[18] Motherboard slots come in a various physical sizes, referenced to the lane count, supporting x1, x2, x4, x8, x16 and x32 lanes

2.6 Lattice ECP2M FPGA

There are two classes of available FPGA devices, namely high-end performance and low-cost . High-end FPGAs spare no expense in offering maximum performance with features such as high clock speeds and DSP blocks while the low-cost camp ignored any spare feature in order to minimize die size and production cost. Lattice Semiconductor bridged the divide on their ECP2M devices by offering SERDES transceivers, increased RAM and DSP blocks which were modeled on their already successful low-cost ECP2 FPGA architecture.

In general, SERDES transceivers become complex and hence expensive when they need to support various protocols and data rates. Lattice SERDES transceivers however only targeted specific high speed applications within the 3Gb/s range such as PCI-Express and gigabit Ethernet [37], thus keeping them low-cost. These devices also include 18 × 18 Multipliers and on-board digital clock managers. Depending on their package size, Lattice FPGAs can be purchased in volume for a less than USD 100 per unit [18].

The user specification [19] for the selection of a suitable FPGA within this family was further constrained to a single FPGA because during the project design stage only the pin allocation table for the ECP2M-35 was available. This was amended in the newer edition of [43]. Lattice provided *Orcad* symbol libraries for the ECP2M-35 which were converted - via the *Mentor Graphics* library converter tool - into *DxDesigner* symbol format. These translated symbols were checked against the pin allocations tables of [43] and corrections were manually edited.

2.6.1 Required FPGA Resources

The summary of the FPGA I/O and resource requirements for the communications between the FPGA and other peripherals is shown in *Table 2.2*.

In order to ease design, the FPGA with the highest I/O count and speed grade within the ECP2M-35 range was selected, specifically the 672-pin fpBGA and -7 speed grade with part number LFE2M35E-7FN672C. In comparison with the device family summary of [43], *Table 2.2* shows that this FPGA has adequate resources for design. The design objective was to adequately allocate the I/O pins and internal FPGA resources for application within the system architecture of *Figure 1.3*.

[19] See Section 1.3

Interface Name	I/O Used	Clock PLL/DLL
QDRII	65	2
ADC08D500 Output LVDS	68	1
ADC Input Control	9	-
ADC Output Status	1	-
ADC Temperature Monitoring	2	-
PLL Control	4	-
SERDES[a]	N/A[b]	2
PCI-Express AUX	8	-
FPGA Configuration	12	-
General I/O[c]	27	-
TOTAL	196	5

[a]Used for PCI-Express
[b]Specialized pins
[c]Used for logic analyzer test points, LEDs and RS232 communications

Table 2.2: FPGA I/O and Resources Requirements

2.6.2 I/O Planning

Lattice ECP2/M devices have eight general purpose programmable banks and a ninth configuration bank documented under *sysIO* in [43]. Each of the eight general purpose *sysIO* banks has a supply voltage, and two reference voltages in order to support multiple signaling standards on a single FPGA. I/O planning was approached by defining the required I/O resources for each peripheral interface and deciding on the FPGA orientation while ensuring the following factors:

- Minimizing the PCI-Express routing length between the back-plane slot and the FPGA
- Making sure the FPGA I/O banks, within the specified orientation, supports the required signaling standard.
- Guaranteeing that individual interfaces can be separated over two adjacent I/O banks, while still maintaining the electrical and switching specifications of each interface. This separation is imperative as simultaneous driving of numerous output pins within the same bank can cause ground bounce and switching noise which can cause destructive interference on nearby sensitive components.
- Limit the number of net cross-overs while routing to ease the next stage of PCB implementation.
- Allowing the relevant input clocks to be routed to the necessary FPGA resources while minimizing clock skew.

The hierarchical X-FPGA symbol of the schematics of *Appendix F* visually encapsulates the decisions taken as to the above-mentioned criteria. The required resources FPGA, together with the FPGA orientation, is presented in relation to peripheral interface connection. The ECP2M also includes special DDR hardware registers on specific banks, especially designed for interface to high speed interfaces such as the ADC and QDRII. Through its operation described in [43], the data rate can be divided down with a proportional increase in data-path width bringing the clock and data speed into the realm of the FPGA logic core. Conventionally, while using the *Mentor Graphics* suite, I/O planning is assisted by *I/ODesigner* in order to achieve a reduction in design cycle time and improve reliability. However, *I/ODesigner* did not include the Lattice ECP2M libraries and thus I/O planning was done manually within *Microsoft Excel* spreadsheets of *Appendix F*. The ECP2M does not provide on-die digitally controlled termination, hence external termination was required. The impact on considering the termination in routing is discussed in *Section 3.1.5*.

2.6.3 Digital Clock Management

Global clocks (primary and secondary) are distributed in the form of eight quadrant-based primary clocks and flexible secondary clocks[20]. Clock sources include clock input pins, internal nodes, PLLs and DLLs. Edge clocks on each edge of the device allow clock fan-out for high speed I/O interfaces across adjacent banks on the same edge with minimal skew and delay[43]. Edge clocks thus allowed the ADC and QDRII interfaces to be split across banks 2/3 and 4/5 respectively. FPGA input clock pins for both Global PLL (GPLL) and Standard PLL (SPLL) require a frequency range f of between 2MHz$<$ f $<$420MHz[21] with a clock jitter period of $< \pm$200ps [43].

The identical system clock network of [41] was implemented using the *Cypress Semiconductor* CY2304 3.3V Zero Delay Buffer with a 100MHz reference clock oscillator. Input-to-output skew and cycle-to-cycle jitter for the CY2304 are guaranteed to be $< \pm$250ps and <100ps respectively. The four CY2304 outputs - specifically designed to distribute clocks in high-performance applications [21] - where traced onto dedicated clock pins.

Outputs clocks of the ADC and QDRII interfaces were routed to global clock pins in order to use the edge clock distribution network.

2.6.4 SERDES/PCS

The ECP2M-35 has one quad embedded SERDES/PCS logic supporting four independent full-duplex data channels where each quad, in turn, supports four independent full-duplex

[20]Primary and secondary clock differences are described in [43]

[21]The lower parameter is dependent on whether an external capacitor is implemented

data channels. Since each quad has its own reference clock - sourced externally from package pins or internally from the FPGA logic - different quads can support different standards on the same chip. In addition, these can be configured through *ISPLever* to support independent industry standard, high speed protocols with a data-rates of up to 3.125Gbps, such as PCI-Express [43]. This flexible feature allows for bridging between different standards within a single device but in terms this design, the entire quad unit is configured as a 4-lane PCI-Express interface. Details of PCS functionality can be found in the ECP2M FPGA datasheet [43] .

2.6.5 Non-Volatile Configuration

The configuration memory within the FPGA is based on volatile SRAM technology and therefore an external non-volatile memory is required to maintain the configuration image when power to the device is lost. The image is loaded into the FPGA on a reset operation or the application of power. ECP2M devices support independent JTAG programming as well as slave modes grouped under the *sysConfig* documentation [43].

The FPGA is reconfigured by uploading a 'bitstream file' into the configuration space. Following this reconfiguration the FPGA functions according to the user specifications as described in the HDL code. Upon entering the configuration mode selected by external pins, the FPGA performs operations of *Figure 2.10.* $INIT, \overline{PROGRAM}, CFG[2:0]$ *and* $DONE$ are physical FPGA pins but have no meaning when using the JTAG configuration port. During configuration, the *INIT* pin becomes an error detection pin. If a ID or CRC error is detected the *INIT* pin is driven low. This gives the design an LED test-point allowing the user to verify that configuration occurred successfully.

JTAG is inherently cumbersome and a time consuming process relative to serial flash. The ECP2M device family is compatible with '25 series' SPI flash memory with configuration in SPIm mode[43]. This allows the flash memory to be split into discrete sections, namely the primary and secondary/golden boot images. The FPGA is loaded with the golden image if there is a failed configuration from the primary boot record. The *ST Microelectronics* M25P64 was selected as it has 8MB of memory and supports the fast-read function allowing the entire memory space to be polled at the maximum clock rate of 50MHz [76]. A reference implementation can be found in [43].

2.7 Debugging Interfaces

Debugging interfaces form a critical part in testing and hardware verification phase of the project.

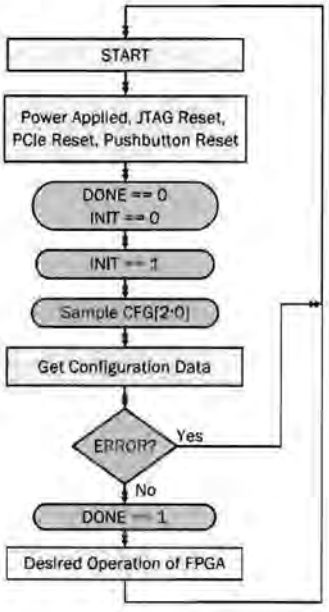


Figure 2.10: ECP2M Configuration Process

2.7.1 LEDs and Test-points

LEDs are designed to be used as a visual debugging, and are connected to FPGA I/O pins. The stability and status of major power supplies is also indicated by the use of LEDs. Test-points of critical voltages and ground connections are strategically distributed around the board to allow for ease in debugging the system.

2.7.2 RS232

RS232 provides reliable, easy to use serial interface for debugging and data transfer. The background and key features in selecting a suitable transceiver is fully documented in [49]. The *MaximIC* MAX3232 dual 120kbps was chosen for its ability to operate at $3.3V$ and only requiring four capacitors for the internal charge pump. RS232 offers a robust method of downloading the captured samples into the PC.

2.7.3 PX6418 Tektronic Logic Analyzer

The design supports the connector for the *PX6418 Tektronic Logic Analyzer*. This connector is connected directly to the a $3.3V$ bank on the FPGA. Care must be taken in writing data as there is no buffer between the analyzer and the FPGA.

2.8 Power Management

The on-board voltage regulation was designed to meet the worst-case current and thermal dissipation requirements as well as provide the necessary voltage sequencing. This section details the design of the power management system.

2.8.1 Estimation

Power estimation was performed by tabulating the worst-case active power usage of each component from their respective data-sheets. In the case of the FPGA, the calculation is non-trivial because of the dependence on dynamic factors such as device utilization, operating temperature and activity factor [43]. Hence, a program called *PowerCalc* - part of the *ISPLever*package - provides the designer with a power consumption overview through its FPGA resource utilization estimator. The over-estimated[22]power requirements of each regulated digitizer voltage is presented in *Table 2.3*. The estimates show that the power requirements to be 1.84W greater than the maximum PCI-Express specification of 25W. External power connectors were therefore added to fulfill the standalone requirement as well as allow for increased power usage through a standard ATX power supply[23]. The full *PowerCalc* spreadsheet appears in *Appendix B*.

Regulated Supply Name	Power Required $[W]$
9V_AMP (9V)	1.86
5VRF (5V)	0.75
3VA3_PLL (3.3V)	0.495
3V3 (3.3V)	3.98
2V5 (2.5V)	5.655
1V9 (1.9V)	1.4[a]
1V8 (1.8V)	2.085
1V5 (1.5V)	4.475
VCC_CORE (1.2V)	5.4907
1V2 (1.2V)	0.65
Over-Estimated Total	26.84 $[W]$

Table 2.3: Worst-Case Power Supply Requirements

[a]This is an exact value from [59]

[22]By a factor of 1.5

[23]For power consumption $\geq 25W$

2.8.2 Distribution

The decision was taken to source the power distribution network (*Figure 2.11*) solely from the PCI-Express 12*V* supply rail. Regulators from the *Texas Instruments POLA* switch-mode range were incorporated in the digital section due to their compact solution for high power designs together with an operational efficiency of up to 90%. Input/Output capacitors were chosen in accordance with [32] for a ripple voltage <0.1Vpp. Linear regulators - with high PSRR - were implemented to regulate power for the analogue circuitry as recommended by [65, 36]. Care was taken as not to exceed the thermal dissipation specifications of each regulator [12, 81]. The 1V9 input was isolated through a ferrite bead as suggested by [40]. Furthermore, any noise sensitive supplies - such as those of the QDRII and FPGA SERDES - were isolated and decoupled as specified in [38].

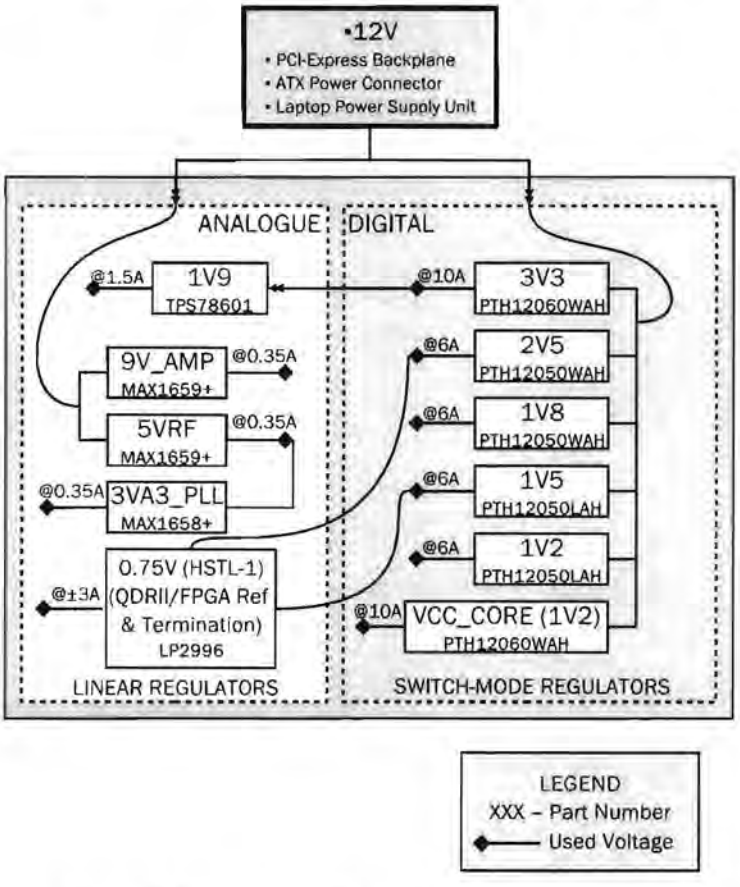


Figure 2.11: Digitizer Power Distribution Network

2.8.3 Sequencing

Voltage sequencing was accomplished through the *Texas Instruments POLA* AutoTrack function and design described in [80]. *Figure 2.12* illustrates the AutoTrack concept. On power-up, a voltage supervisor (namely the *Texas Instruments* TL7712A), generates a

power on reset. After a delay t_d - corresponding to an adjustable RC delay - the outputs of the PTH modules follow a ramp ($Vcontrol1$) function stopping at their respective setpoints (dictated by the output voltage setpoint resistor). From *Figure 2.12* voltages reach their setpoints after delays t_{1-5}. When the 3V3 POLA module reaches its setpoint at t_4 , the ramp ($Vcontrol2$) for the 1V5 supply is triggered. The voltage sequencing design ensured that:

1. The FPGA core voltage reached its minimum voltage value before the auxiliary and configuration banks reached their minimum supply values [43].
2. With respect to the QDRII, VDD came up before VDDQ.

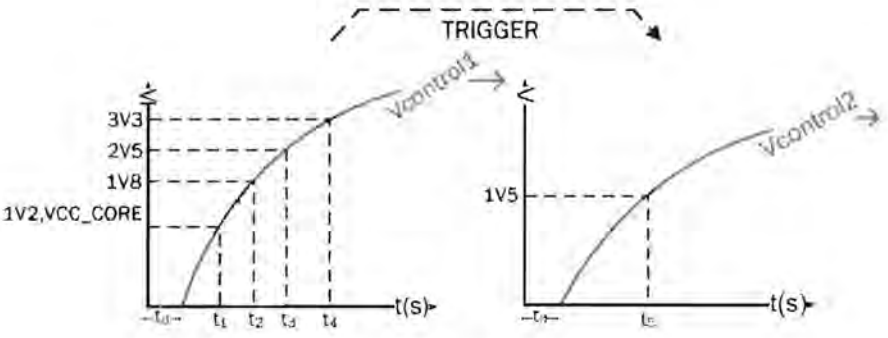


Figure 2.12: Add-in Card Power Sequencing

2.9 Chapter Summary

The chapter commenced by outlining the principles of wide-band conversion, with a view to understanding the criteria for ADC specification, in terms of integration into the HSHS. A survey of commercially available OTS ADCs produced two potential candidates and after a comparison, the *National Semiconductor* ADC08D500 was selected as the HSHS digitizer on the basis of its superior performance characteristics. A functional description of the ADC was given, showing the design implementation. This ADC requires a full scale analogue differential input of ≈750mVpp while in Extended Control Mode (ECM) and thus the problem of transforming the 1Vpp input signal[24] was addressed. BALUN TLTs - with their lower distortion and power consumption - were used to preform the single-ended to differential conversion required for the A-D inputs. *Octave* simulations of BALUN transmission line equations predicted the required input voltage, thus allowing for the attenuator/gain system to be fully designed. The simulations showed that in order

[24]Refer to Section 1.3

to maximize the FSR, a single-ended signal of amplitude $\approx 1.5V_{pp}$ into 50Ω was needed at the BALUN input. The Analogue Front End - consisting of a cascaded attenuator and gain block - was thus designed with necessary voltage gain transformation of 3.45dB. A critical aspect of sampling performance, namely clock jitter, was then introduced. Jitter on the sampling clocks results in sampling voltage errors which degrade the overall system SNR. The allowable clock jitter - so that the noise level does not increase above $\frac{1}{2}LSB$ - was calculated to be 2.44psRMS with an SNR_{total} of 46dB. The ≈500MHz frequency synthesizer - consisting of a PLL, Loop Filter and VCO - was designed to meet these specifications. *WebBench* simulations confirmed that the frequency synthesizer topology has a total jitter of 1.88psRMS, closed loop bandwidth of 33.45kHz, phase margin of 47.18 degrees and an equivalent spur power of −47.641dBc. According to *Equation 2.6*, the maximum allowable f_a - before SNR_t is sacrificed below its recommended value - is calculated to be ≈420MHz. Sampling with $f_a = 1.5GHz$ the SNR_t is calculated to be as low as ≈35dBc.

Attention was then diverted away from analogue to digital design:-

Several high-speed architectures were reviewed but due to its optimization for buffering/cache applications with a unity read/write ratio as well as only 5ns latency and no bus-turnaround time, QDRII was selected as the best suited high-speed memory for the HSHS Digitizer. The design considerations in QDRII implementation were presented.

An overview of the PCI-Express interface followed, along with the usage of auxiliary signals and power specifications taken into account in design were outlined and described.

The user specification [25] for the selection of a suitable FPGA within this family was further constrained to a single FPGA because during the project design stage only the pin allocation table for the ECP2M-35 was available. In order to ease design, the FPGA with the highest I/O count and speed grade within the ECP2M-35 range was selected, specifically the LFE2M35E-7FN672C. This FPGA was shown to have adequate resources for the design. The I/O pins and internal FPGA resources for application within the HSHS architecture were successfully allocated with respect to the itemized criteria. The configuration memory within the FPGA is based on volatile SRAM technology and therefore an external non-volatile memory, namely the *ST Microelectronics* M25P64, was required to maintain the configuration image when power is lost to the device.

Debugging interfaces were briefly described, but form an integral part of hardware verification.

Finally, the on-board voltage regulation was designed to meet the design's worst-case current and thermal dissipation requirements as well as provide the necessary voltage sequencing. Power estimation was performed through tabulating the worst-case active

[25] See Section 1.3

power usage of each component from their respective data-sheets. In the case of the FPGA, the non-trivial calculation was estimated through *PowerCalc*. The over-estimated[26] active power requirements was calculated as 1.84W more than the maximum consumption of 25W specified by the PCI-Express Specification. External power connectors were therefore added to fulfill the standalone requirement as well as allow for increased power usage through a standard ATX power supply. The *Texas Instruments POLA* switch-mode regulator range were incorporated in the digital section due to their compact solution for high power designs together with an operational efficiency of up to 90%. Input/Output capacitors were chosen in order to achieve a ripple voltage <0.1Vpp. Furthermore, any noise sensitive supplies - such as those of the QDRII and FPGA SERDES - were isolated and decoupled. The issue of voltage sequencing design ensured that:

1. The FPGA core voltage reached its minimum voltage value before the auxiliary and configuration banks reached their minimum supply values [43].
2. With respect to the QDRII, VDD came up before VDDQ.

[26]By a factor of 1.5

Chapter 3

System Implementation

This chapter is separated into two sections that detail the implementation phase of the project covering the areas of:

- **PCB Implementation** - describes the process of transforming the schematics into a physical PCB. Issues of layering, formulating the routing constraints from the manufacturer specifications, component placement and planing are discussed. Post-Route Board Simulations are performed and interesting effects are presented along with the resulting solutions and design adjustments.
- **Firmware Implementation** - gives an overview of the methodology for programming the FPGA followed by an explanation of the firmware required for the digitizer's integration into the HSHS.

3.1 PCB Implementation

The schematics were imported into *PADS Layout* through *DxDesigner Link*. Errors occurred during this procedure because of incorrect symbol and footprint definitions. These cascading errors[1] were cleared through an iterative process of fixing a single error and re-importing the entire design until all the errors were cleared. Components decal/footprints were either sought out from the free libraries offered by *PCB Libraries Inc.*[2] or in the internal *PADS Layout* libraries. The integrated decal/footprint editor was only used if the footprint did not exist in either of these libraries. CAM documentation is presented in *Appendix F*.

Maximizing signal integrity while reducing Electro-Magnetic Interference (EMI) in high-speed signals was viewed as a high design priority and therefore special attention was

[1] Fixing one error had the effect of fixing numerous other errors
[2] See PCB Libraries, Inc. `http://www.pcblibraries.com/`

directed at those areas which were considered to be high risk. *Hyperlynx*, a software package from *Mentor Graphics*, was used to simulate the signal integrity and EMI performance of the *AstroGIG*. The two aspects of *Hyperlynx*, *LineSim* and *BoardSim* allow the user to firstly simulate a schematic entry transmission line and secondly, to simulate the entire routed PCB layout.

3.1.1 Supporting Local Business

In an effort to support local business, only South African based companies were used in the production of the *AstroGIG* digitizer. It was also considered easier to engage in business transactions with locally based companies as opposed to an overseas manufacturer because of time-zone differences and the language barrier. Added to this was the benefit of keeping costs down by not having to pay import/delivery charges. The two companies that offered the cheapest prices where *Trax Interconnect*[3] and *Tellumat*[4] for PCB manufacture and assembly respectively.

Information extracted from *Trax's* production specifications set the layering, routing and placement constraints to which the PCB could be implemented.

3.1.2 Add-in Card Dimensions

PADS layout did not provide an adequate tool to draw the board outline and therefore it was created by Willem Esterhuyse (KAT researcher) in *AutoCAD*[5] and imported into *PADS*. The required keep-outs and mounting holes were added in *PADS* according to the PCI-Express add-in card specifications [71]. The implementation originally commenced with the use of the maximum size, full length, standard height mezzanine form factor card profile with dimensions specified in [71]. However, a recommendation was later found that standard height add-in cards be designed with a maximum length of 9.5inches due to the fact that some motherboards do not support long-profile cards [71]. Through an approximate first order component placement exercise it was seen that the *AstroGIG* had to have a length of $\leq$ 10.84inches.

3.1.3 Layer Specification

FR-4 material both the most commonly used PCB fabrication material and the most cost effective [25], suitable for a design operational frequency of $\leq$2GHz. At 500Hz the dielectric constant of FR-4 is rated as 4.35. At $\geq$2GHz, reflections and losses severely

[3] *Trax Interconnect www.trax.co.za*

[4] *Tellumat www.tellumat.com*

[5] The outline was saved as a **.dxf* file format

degrade the signal. PCI-Express operates at 1.25GHz and [71] explicitly states that the electrical specification is optimized for implementation on FR-4 material. *Figure 3.1* shows the *AstroGIG* 8-layer stack-up on FR-4 which satisfies the PCI-Express add-in card maximum thickness of 67mils [71] as well as being chosen from the list of *Trax Interconnect* standard lay-up tables. The 8-layer stack-up is divided into a configuration whereby each signal layer is shielded by at least one reference plane, reducing crosstalk and increasing signal integrity. A lower layer count stack-up could not be used as *Trax Interconnect* does not currently support micro-via technology and therefore BGA fan-out was limited to through hole vias.

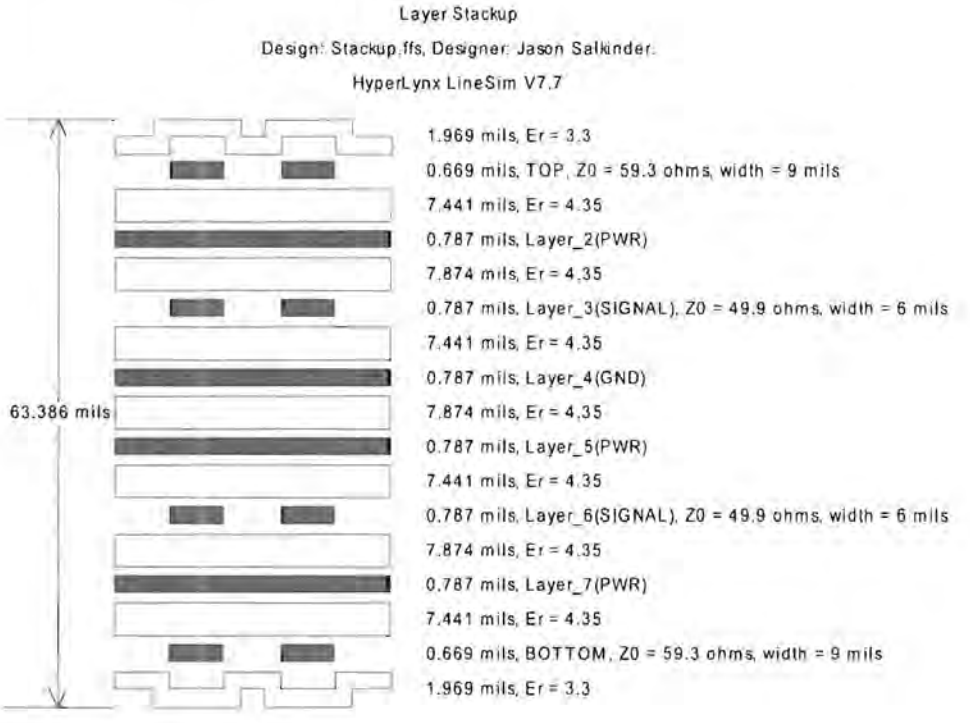


Figure 3.1: *AstroGIG* 8 Layer Stack-up

3.1.4 Formulating the Routing Constraints

Routing rule constraints for both manual and auto routing were established in-conjunction with *Trax's* short-form specification and the relevant stack-up data was entered into *LineSim*:

3.1.4.1 Impedance Matching vs. Trace Dimensions (Single-Ended)

In order to avoid signal reflections[6], impedance matching attempted to keep single-ended trace impedance as close to 50Ω as possible. Various routing iterations showed a trade-off between what the specifications allowed and what the design required with the major factor being the minimum via size for BGA fan-out. In order to achieve routing underneath the BGA - on the top and bottom signal layers - the trace width had to be ≤9mils which in turn resulted in $Z_0 \geq 59.3\Omega$. The final trace widths and corresponding characteristic impedances' for all layers can be seen in *Figure 3.1*.

3.1.4.2 Length Matching

The routing of grouped nets (e.g.: QDRII Output Data Lines) required all the signals to arrive approximately at the same time with minimal skew and delay for clocking. This is highly dependent on length matching within the group, signal rise/fall time and board material. The length matching (*lengthgrouped*) maintained less than $\frac{1}{10}th$ of the effective operating wavelength which can be mathematically expressed as:

$$lengthgrouped < \left(\frac{1}{10}\right)\left(\frac{cT_r\varepsilon_r}{0.35 \times 7}\right)[m] \tag{3.1}$$

where T_r is the signal rise/fall time, ε_r is the FR-4 dielectric constant and c the speed of light in a vacuum. *Equation 3.1* was manipulated from the termination rules given in [7].

3.1.4.3 Routing Topology

The routing topology is mainly used in the auto-route process and determines the pin-to-pin order when routing a net or moving a part. The simplest routing of 'minimized' was employed on all net groups except for the QDRII nets where 'serial source' was selected to properly route the HSTL-1 terminating resistors [53]. The topology also had to minimize the amount of routing corners/bends[7], vias and layer changes.

3.1.4.4 Differential Pairs

The impedance of the differential pairs was kept as close to $100\Omega \pm 10\%$ as required by the LVDS signaling standard [47]. Trace widths and conductor separations for signal routing layers - *Figure 3.2* - were calculated in *LineSim*. According to [30], tight coupling

[6]Most manufacturers specify component input/output impedance to match a 50Ω environment.
[7]Optimal corner angle was specified as >90 degrees

between pairs and increased spacing to other nearby pairs aids to minimize crosstalk and EMI. The optimal specification for LVDS coupling and routing is fully documented in [47]. The width and separation were set to $(6,6)$ and $(5,7)$ for outer and inner layers respectively. Further restrictions were placed on the PCI-Express pairs routing according to the PCI-Express PCB implementation guidelines of [30].

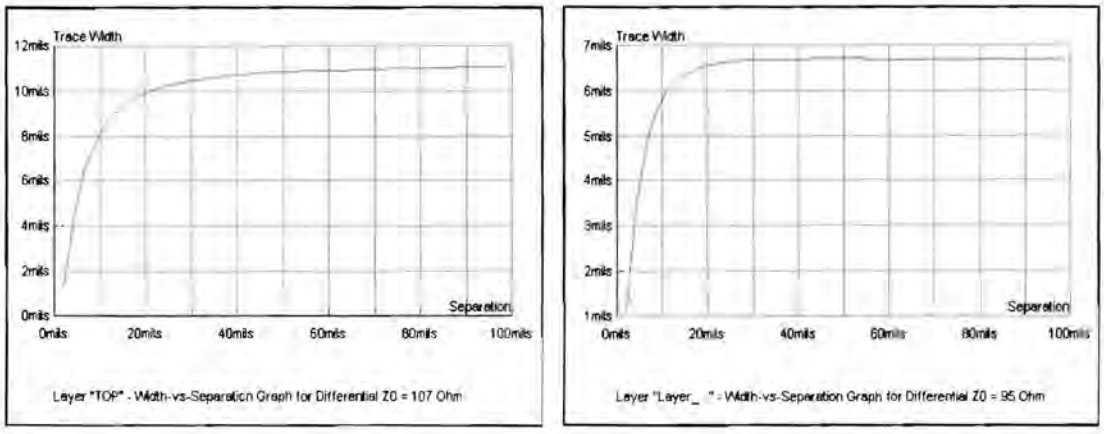


Figure 3.2: *AstroGIG* Differential Trace Width vs. Trace Separation Plots

3.1.5 Component Placement

The first placement task was to isolate the analogue and digital components. Stray capacitance within the ADC package allows coupling of noise from switching digital currents into the analogue circuitry. This distinct separation prevented signal mixing and degradation of the A-D performance [82] because even if specific modules are properly isolated within themselves, the neighborhood in which they exist can add destructive interference [35, 79]. Switch-mode supplies were thus located physically and electrically far away from any analogue circuitry.

The next requirement was to shift these components in such a way as to minimize the routing distance of high-speed signals and limit the number of 'rats nest' crossovers. Pin-swap attributes were added to symbol definitions in order to help the routing process and untangle the rats-nest. Terminating resistors for both the LVDS and HSTL-1 lines were placed as close as possible to their respective end-points. The basic layout for LVDS pin pairs in ECP2M device created further discontinuities as differential pairs pins are not located adjacent to each other on the physical package. In comparison, *Xilinx* devices have optimized this layout and routing strategy, combining adjacent pairs as well as on die termination. In the case of the ADC08D500 outputs, terminating resistors were placed within 0.5inches of the ECP2M pins as recommended by Lattice Engineers on their development board.

3.1.6 Power Planing

As there are various supply voltages required for the *AstroGIG* system, the four plane layers of *Figure 3.1* were divided into physically separated areas, allowing voltages to be distributed across the PCB.

Due to the Proximity Effect, high frequency signals tend to return in the path of least inductance, which generally is on the reference plane directly underneath the trace carrying the forward current [82]. Routing high speed signals over partitioned plane boundaries - without proper decoupling and current return path - can create a dipole antenna effect which can negatively impact SI performance [64]. The issue of return current paths for the minimization of EMI was solved through (as per the suggestions of [82, 64, 27, 66]):

- **Solid Ground Plane** - Layer 4 (*Figure 3.1*) was selected as a solid ground plane.
- **Separating Analogue/Digital References** - Reference planes (Layers 2, 5 and 7 of *Figure 3.1*) were primarily partitioned underneath the A-D[a].
- **Routing Discipline** - Analogue/Digital signals were only routed on their respective board sections. The Proximity Effect helps in design because no return currents will mix into the separate section if there is a clear separation and no routing crossovers. Board layout thus also has a major bearing on the limiting crosstalk.
- **Distributed Decoupling** - Allows return currents on distributed planes to easily enter the ground plane and return to the driving source.

---

[a] – Recognized as the boundary between analogue and digital sections

One exception to these rules was that the QDRII routing crossed a reference plane boundary because of the planed HSTL-1 reference voltages seen on Layers 2 and 5 of the CAM documentation given in Appendix F.

3.1.7 Post-Route Board Simulation (*BoardSim*)

Simulation requires selected components to have an electrical characteristic model. I/O Buffer Information Specification (IBIS) models - specified in [58, 56, 78] - were used in *BoardSim*. Parameters such as board voltages and passive componet values also had to entered into the simulator. *Figure 3.3* illustrates an example of a trace ready for simulation. In some cases the *BoardSim* routes were exported to their equivalent *LineSim* transmission lines as it was considered simpler to analyze.

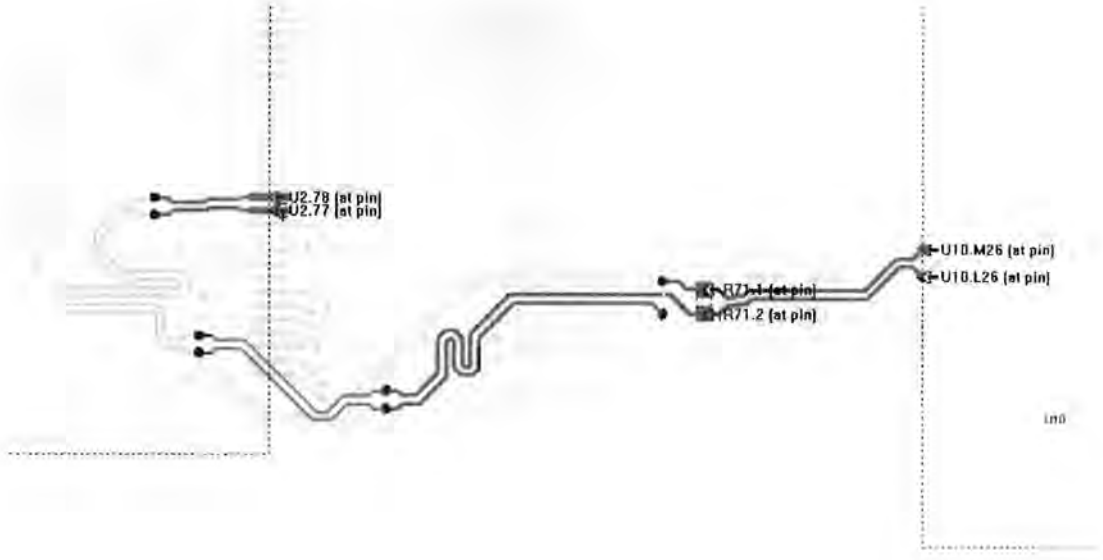


Figure 3.3: Trace Between the A-D and FPGA Ready for *BoardSim* Simulation

3.1.7.1 ADC LVDS

Figure 3.4(2), shows that the clock signal is non-monolithic between trip points[8] which might cause a clocking error in the data line of *Figure 3.4(1)* . When the same traces were simulated using an equivalent *Xilinx* device, the waveform became a clean clock signal. Under close inspection of the IBIS models, it was found that this unexpected behavior was caused by the difference between the internal rise/fall times of the FPGA and ADC pins. The ECP2M and National A-D have a rise time of 0.9V/ns and 1.13V/ns respectively. This disparity caused reflections resulting in the non-monolithic behavior. In order to compensate and 'slow down' the ADC output clock, a 10pF capacitor to ground[9] was placed as close as possible to the DCLK source. As the slew rate is governed by $i = C\frac{dV}{dt}$, the increased capacitance decreased the rise/fall time proportionally which can be seen in *Figure 3.4(3)*.

3.1.7.2 QDRII HSTL-1

The QDRII clock exhibited the same behavior around the HSTL-1 trip points[10] as the ADC DCLK. Compensation capacitance was added and the resulting waveforms are presented in Figure 3.5.

[8]The trip points for the LVDS signals are 0.1V and -0.1V [47]
[9]Essentially a Low Pass Filter (LPF)
[10]The trip points for the HSTL-1 signals are 0.65V and 0.85V

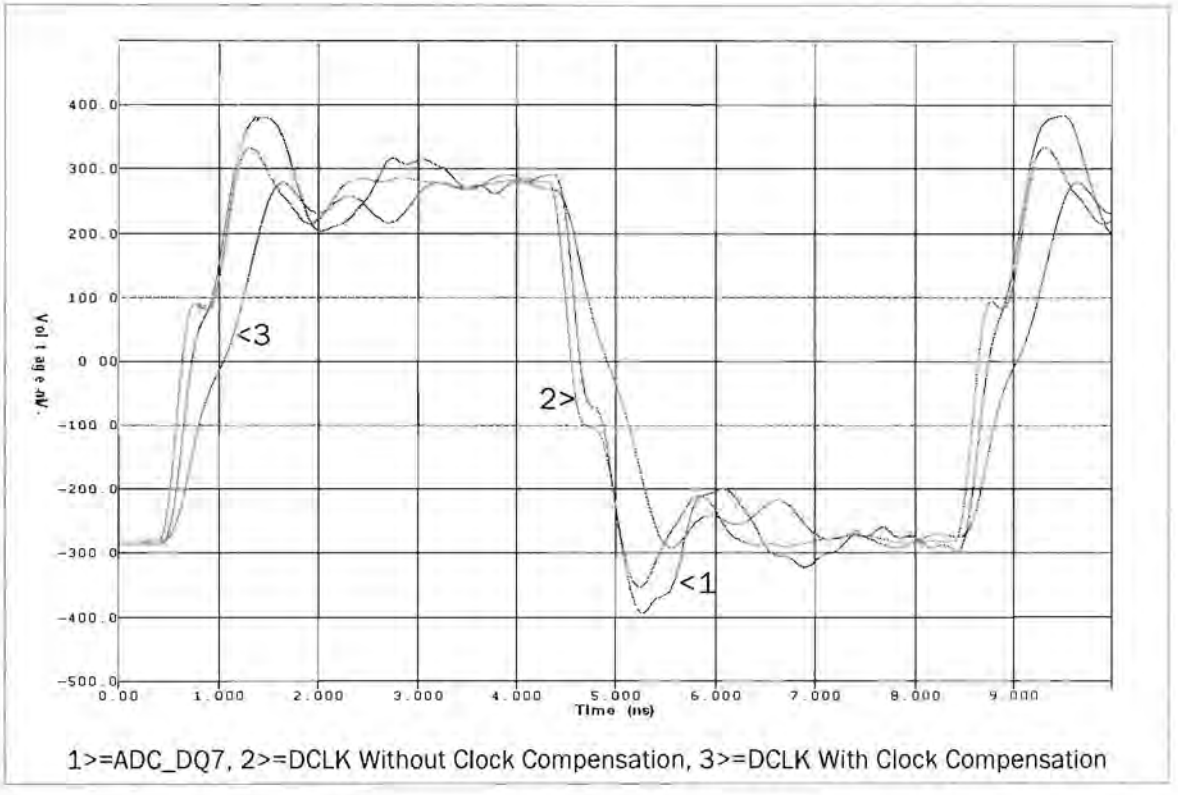


Figure 3.4: Simulation of ADC DCLK and Data Line DQ7

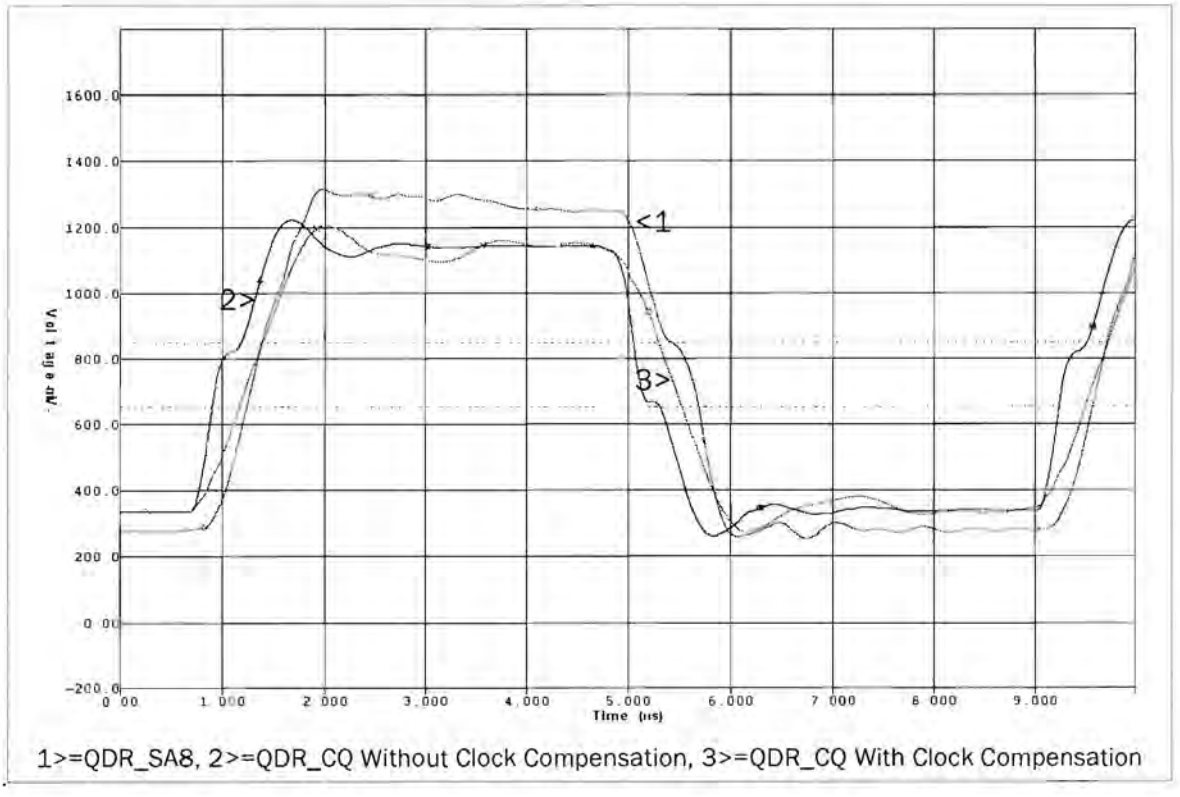


Figure 3.5: Simulation of Data Line QDR_SA8 and Echo Clock QDR_CQ

3.1.7.3 PCI-Express LVDS

PCI-Express Simulation was performed with help from the *Hyperlynx PCI-Express SI Analysis Design Kit* which covered:

1. Analyzing loss on transmission lines in terms of *dB*
2. Transmitter specification compliance
3. Effects of loss on received eyes
4. Crosstalk
5. De-emphasis

Pre-designed eye-diagrams for both transmitter and receiver were included in the kit. The receiver in both instances was modeled as two 50Ω resistors to ground [70]. Eye-Diagrams from the transmitting and receiving differential pairs for the first of the four lanes is shown in *Figures 3.6* and *3.7* respectively. The simulations were also performed under maximum Gaussian jitter of 0.4UI [70] in which the eye still remained sufficiently open. Capacitance added by physical connector pins[11] would increase signal rise/fall time thus closing the eye. However, it was considered fair to assume the severity of this eye deterioration would not cause bit errors. Line-loss was shown to be less than the allowed 13.2dB as specified in [70]. The *Design Kit* recommended that PCI-Express LVDS pairs be routed with minimal length and sufficient inter-pair spacing as this provided the most effective method of reducing crosstalk. Routing was therefore revised as to have each link outside the coupling region of any adjacent pair. De-emphasis analysis could not be carried out as neither the required packages of *Eldo* nor *HSpice* were installed.

3.1.7.4 Batch Simulation

The definition of grouped nets in *Hyperlynx* differs from the routing rules constraints expressed in *PADS Layout*. Groups within *Hyperlynx* are defined by coupling region and therefore simultaneous oscilloscope simulations on nets outside the selected coupling region cannot be preformed. Batch simulation allows the SI performance of any amount of nets on the entire PCB to be calculated in a single iteration. Performance was checked against parameters such as overshoot, rise time, delay, etc. as detailed in [52] with the results either being that of passed or failed. Each failure was investigated until so that it could be cleared. *AstroGIG* passed all batch simulation testing for all high speed routes. Timing margins for firmware design can also be derived from these simulations [52].

[11] Instead of the 50Ω resistors to ground

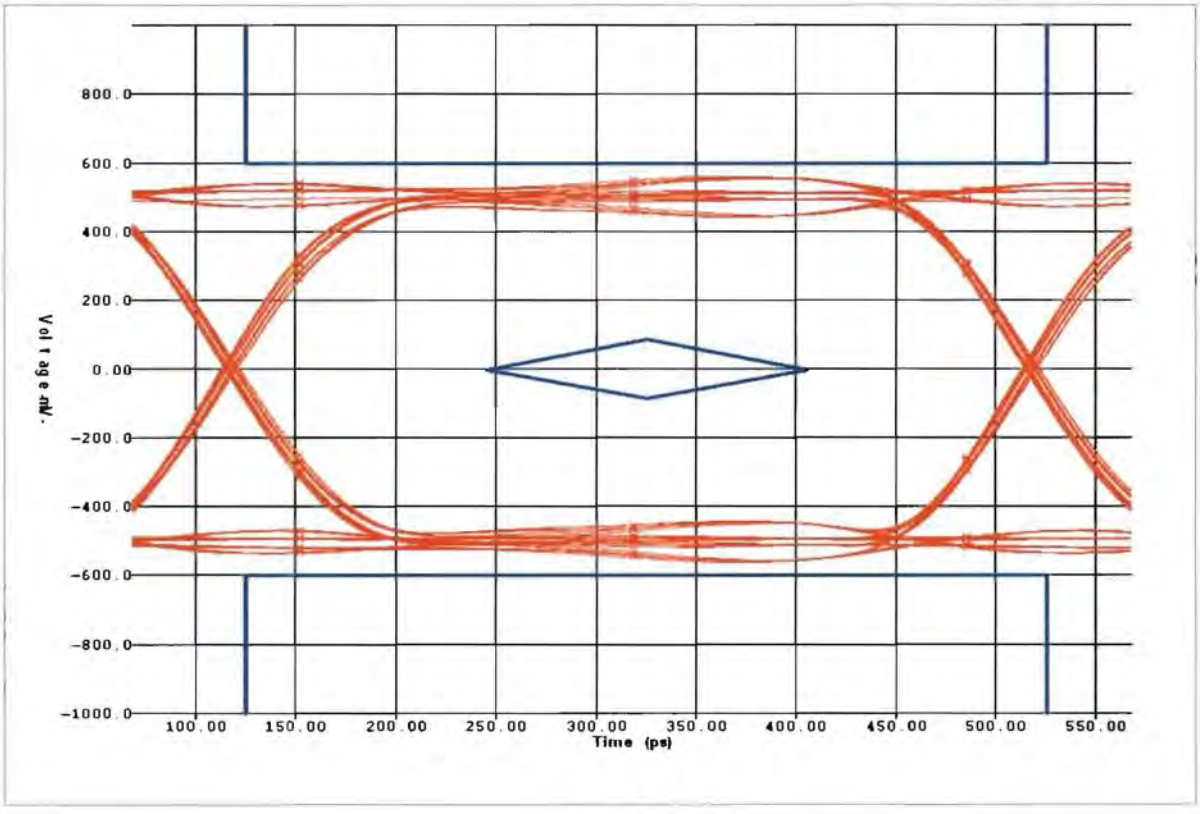


Figure 3.6: Eye-Diagram Simulation of PCI-Express Differential Pair *PET_0*

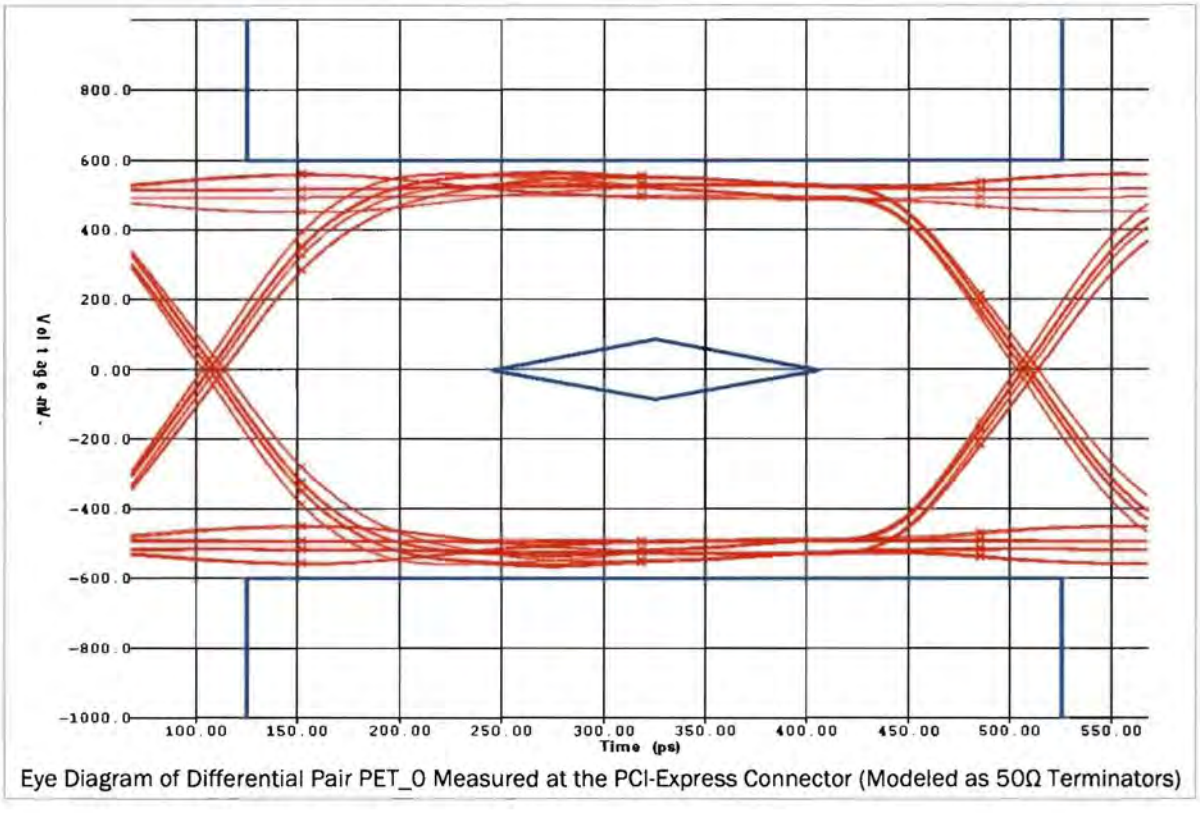


Figure 3.7: Eye-Diagram Simulation of PCI-Express Differential Pair *PER_0*

3.1.8 Completed Hardware

Before production, the final design was checked against the *PCI-Express Add-in Card Checklist* of [11]. Components were procured from the distribution companies of *Digikey, EBV* and *Mouser* or as samples from the various manufacturers. A rough summary of the costs incurred for component procurement, manufacture and assembly of 1x *AstroGIG* are given in *Table 3.1*[12]. These cost would decrease significantly if the boards were mass produced. In comparison, an OTS unit with similar functionality would cost approximately USD 3500 [28] or ZAR 26600 [13]. It can therefore be seen that the *AstroGIG* is capable of competing with these units in a cost sensitive environment.

Major Components/Item (Each)	Cost (ZAR)
ADC08D500	1842.00
LFE2M35E-7FN672C[a]	$\approx$ 1500
K7R321882C	325.00
Others[b]	$\approx$ 1000
Passive Components[c]	$\approx$ 2000
Manufacturing at *Trax Interconnect* (excl. VAT)	2174.48
Assembly at *Tellumat* (excl. VAT)[d]	11,396.60
Grand Total (excl. VAT)	R20238.08

Table 3.1: Rough *AstroGIG* Costing Analysis for Manufacture and Assembly of $x1$ PCB

[a]The FPGA was procured as a free sample

[b]These include the *Minicurcuits GALI-4+, TCCH-80+ and TC1-1-13M+* as well as the oscillators for the *CY2304* and *LMX2313U*.

[c]Such as resistors, capacitors, inductors and ferrites etc.

[d]Including Laser-cut Stencil Top and Bottom, X-rays for BGA and Non-recurring engineering fee

Figure 3.8 and *3.9* shows images the PCB top and bottom component side before soldering. Figure 3.10 shows the fully populated *AstroGIG* Digitizer. X-Rays were taken of the underside of the BGA packages to ensure placement. *Tellumat* also required fiducials for correct alignment by the pick and place machines cameras.

3.2 Firmware Implementation

The firmware was coded in VHDL within *ISPLever*, synthesized with *Precision Synthesis* and finally verified through simulation in *ModelSim*. *ispVM* - the Lattice programming tool - was used to configure the FPGA.

[12]Components not listed were procured as free samples from the respective manufacturers

[13]As per the exchange rate on 15/05/08 of USD 1 = ZAR 7.6

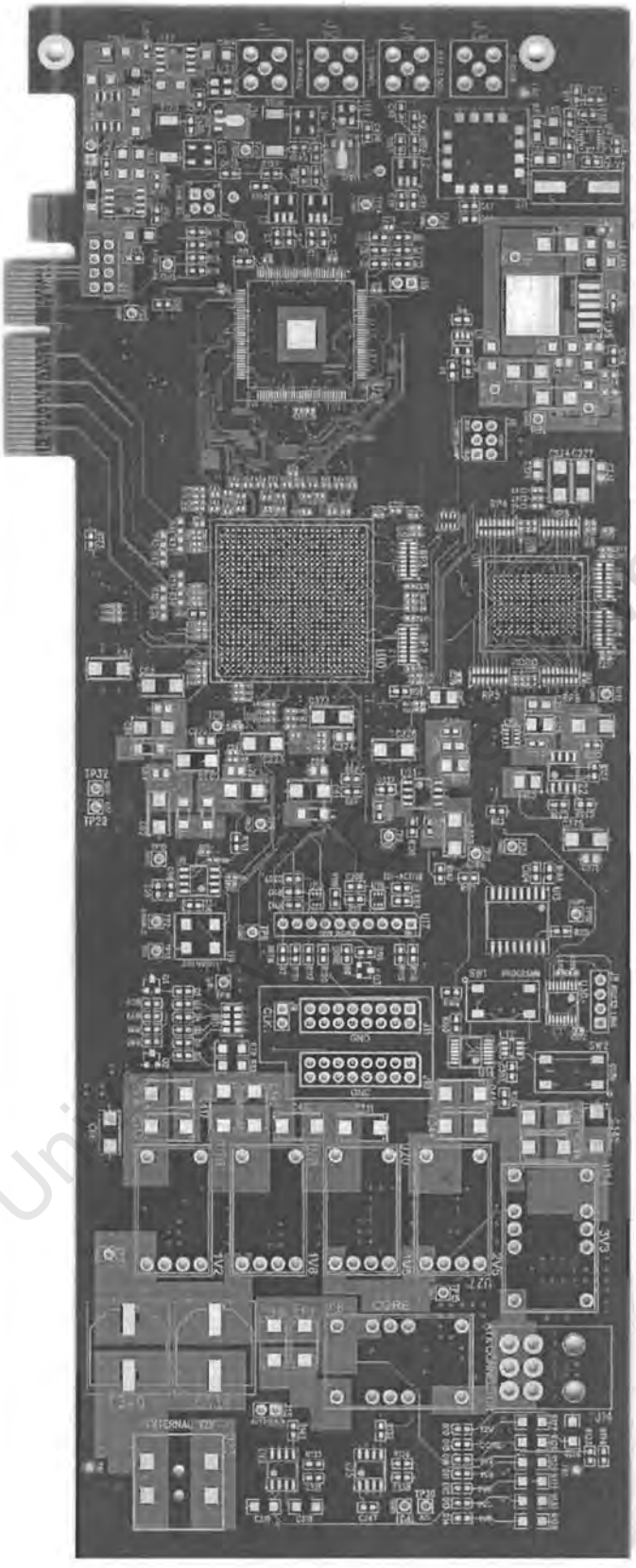


Figure 3.8: Top Component Side Before Soldering

Figure 3.9: Bottom Component Side Before Soldering

Figure 3.10: Fully Populated *AstroGIG* Digitizer

3.2.1 Programming the FPGA

Once the software tools were installed, the methodology of programming the FPGA is as follows:

1. Before start-up, keep in mind the configuration operation (ie: SPI, JTAG) wished to be selected by jumper J6 and place jumpers accordingly.
2. Power up the board making sure that all power LEDs (D10 to D16) are on.
3. Attach the *ISPLever* programming cable to jumper (U17) and ensure that D7 is off.
4. Start *ispVM* and select scan chain. The scan should find the ECP2M device. If there is an error check that the Lattice driver for the programming kit is installed, the programmer is properly connected and if the board power specifications are correct.
5. Once the device is found, a configuration file (*.bit) - generated by the *ISPLever* tools - needs to be loaded into the FPGA. Select the associated file as well as the device access options (as per step 1). It is good practice to make sure that the system is refreshed through the configuration process operation.
6. Press the 'Go' button in the toolbar. D9 should flash during configuration.
7. Once completed, a success report for the programming operation in generated. If an error occurs (also indicated by D8), repeat all the above steps as numerous dynamic faults can cause an unsuccessful configuration.

3.2.2 HSHS Integration

In order to satisfy the functional requirements of the project integration, the firmware modules of *Figure 3.11* needed to be designed. The LVDS I/O Buffers, DDR registers and FIFO modules were generated as a mega-functions in the *IPexpress* tool of *ISPLever*. Modules 8 and 9 *(Figure 3.11)* are necessary for full 'data-streaming' functionality and HSHS integration, however they do not form part of the requirements for this project. The source code can be found in *Appendix* F.

In terms of this project scope, the firmware modules *(Figure 3.11)* - for data capture and transmission to a PC for processing - operates as follows:

- On start-up, the configuration controller first configures the LMX2313U with the necessary control words.

- After about $1sec$ delay, the ADC is configured.
- The system then waits until the until the PLL is locked, indicating stability of the ADC output clock[14].
- With the PLL locked, the ADC LVDS outputs pass through input LVDS I/O buffers and then onto the specifically designed 1:4 gearing ratio DDR hardware registers. This process increases the data width to 64 bits by slowing down the data rate to a manageable 62.5MHz.
- The data is then clocked into the awaiting FIFO which is capable of storing 32768 samples. This is equivalent approximately $1\mu s$ of time resolution sampling at 500MSPS.
- Once the data-set has been captured, the first sample word is read out of the FIFO into the Buffer Controller. The internal structure of the DDR registers places samples in a non-sequential order. Therefore the buffer controller decodes the DDRs manipulation and sends sequential samples to the UART.
- Each of the 8 bytes within the Buffer Controller is then sent to the UART which serially outputs the data to the awaiting PC.
- When the Buffer Controller has sent all the bytes, the FIFO is clocked and the previous 2 steps are repeated until the FIFO empty flag is asserted.

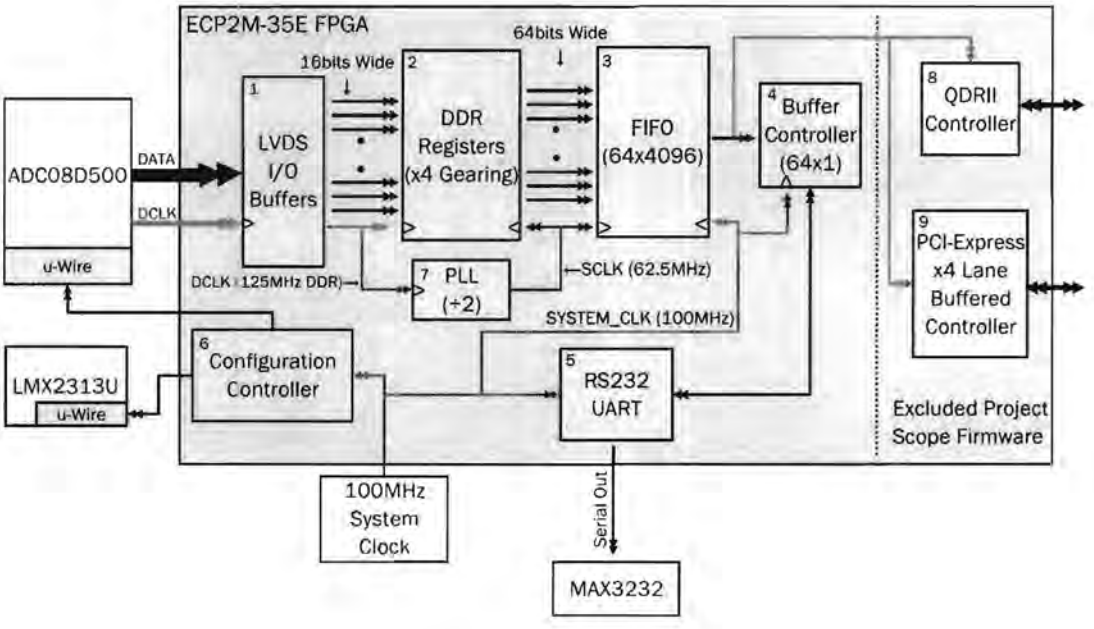


Figure 3.11: Firmware Modules for HSHS Integration

[14]This is directly related to the stability of the ADC sampling clock.

3.3 Chapter Summary

This chapter focused on the implementation of the project in two phases:

PCB Implementation: The schematics were successfully imported into *PADS Layout* with the board outline being created in *AutoCAD* and imported ito *PADS*. South African based companies were selected to manufacture and assemble *AstroGIG*, namely *Trax Interconnect* and *Tellumat* respectively. Through an approximate first order component placement exercise it was seen that the *AstroGIG* had to have a length of $\leq$10.84inches. *Trax's* production specifications set the layering, routing and placement constraints to which the PCB was implemented.

An 8-layer FR-4 configuration - whereby each signal layer is shielded by at least one reference plane - was chosen as it satisfied the PCI-Express add-in card specifications as well as being chosen from the list of *Trax Interconnect* standard lay-up tables.

Routing constraints were then formulated in-conjunction with *Trax's* short-form specification and the relevant stack-up data entered into *LineSim*. Single-ended trace widths had to be $\leq$9mils on top and bottom signal layers in order match the impedance to as close to 50Ω as possible while still ensuring proper BGA fan-out. The length matching maintained less than $\frac{1}{10}th$ of the effective operating wavelength. The simplest routing of "minimized" was employed on all net groups except for that of QDRII nets where "serial source" was selected to properly route the HSTL-1 terminating resistors. Differential pair impedance's were kept as close to $100\Omega \pm 10\%$ with differential width and separation was set to $(6,6)$ and $(5,7)$ for outer and inner layers respectively.

Component placement isolated analogue and digital devices as well as minimized the routing distance of high-speed signals while still limiting the number of 'rats nest' crossovers. Terminating resistors were placed within 0.5inches of the ECP2M pins as recommended by Lattice Engineers on their development board.

Various supply voltages were planed and distributed across the PCB while ensuring a solid return current path.

Visual/Oscilloscope simulations were performed on all critical nets using IBIS models in *BoardSim*. Simulation models were investigated to explain the the non-monolithic clock behavior of the ADC and QDRII waveforms about their corresponding I/O trip points. The cause was found to be related to difference between the internal rise/fall times of the FPGA and ADC/QDRII pins. In order to compensate and 'slow down' the output clock, a 10pF capacitor to ground was placed as close as possible to the clock source. As the slew rate is governed by $i = C\frac{dV}{dt}$, the increased capacitance decreased the rise/fall time proportionally. The PCI-Express interface was tested with help from the *Hyperlynx PCI-Express SI Analysis Design Kit*. Finally, batch simulations were performed to calculate SI performance of the entire PCB in a single iteration.

Before production, the final design was checked against the *PCI-Express Add-in Card Checklist*. A rough estimate showed that it would cost approximately ZAR 20000 to build a single *AstroGIG*. In comparison, an OTS unit with similar functionality would cost approximately ZAR 26600 [28]. It was therefore shown that the *AstroGIG* would be capable of competing with these units in a cost sensitive environment.

Firmware Implementation: The methodology in programming the FPGA in order to get it 'up and running' using the Lattice Software was listed followed by an illustration and explanation of the modular firmware design for HSHS integration.

Chapter 4

Verification and Results

This Chapter discusses the tests performed on the final system to validate categories of both hardware functionality and analogue performance. The obtained results are discussed and analyzed.

4.1 Functional Tests

Functional tests determine the system's capability of performing the functional requirements in order to satisfy the project scope or in other words, serve to prove that the system does what is expected.

4.1.1 General System

Prior to power application, components were checked as to their orientation, polarization and pin-out specifications. The high resistance between power planes confirmed that there were no internal power shorts. Finally a visual inspection ensured that all the jumpers and connector were in their correct position.

4.1.1.1 Power Supplies

The power supplies were checked with a multimeter and shown to be within $\pm 1\%$ of the specified voltage setpoints. The *AstroGIG* consumed $\approx$14W during full operation. This was 11W and 12.84W less than the maximum power consumption specified in the PCI-Express Standard [70] and the overestimated power consumption of *Table 2.3* respectively.

4.1.1.2 JTAG/Flash FPGA Programming

The procedure of programming the FPGA[1] was successfully completed with both SPI and JTAG operations. A LED flasher *.bit configuration file - which toggled a single LED according to an overflow counter connected directly to an input clock pin - was loaded into the FPGA in both instances.

While in SPI operational mode, the PSU was turned off and the programming cable disconnected. When the power was re-applied, the FPGA was programmed through the on-board SPI flash, resuming its LED flashing operation.

4.1.1.3 Pushbotton Resets

Using the same LED flasher configuration, the program could be held in reset mode and the FPGA could be re-programmed by pushing SW1 and SW2 respectively

4.1.2 3-Wire Serial Interface (PLL and ADC)

The 3-wire serial interfaces (PLL and ADC) were probed to see if the firmware - presented in *Appendix F* -correctly configured these devices.

Figures 4.1 and *4.2* show the latching of the 1^{st} 22-bit word into the *LMX2313U*. The data (HEX"60190") was clocked MSB first during the middle of the bit cycle in order to maximize timing margins. Latch-Enable (PLL_LE) was shown to be asserted in accordance to the devices timing waveforms [57]. The waveforms of the the 2^{nd} and 3^{rd} words are not shown but appear in *Appendix F*.

[1] See *Subsection 3.2.1*

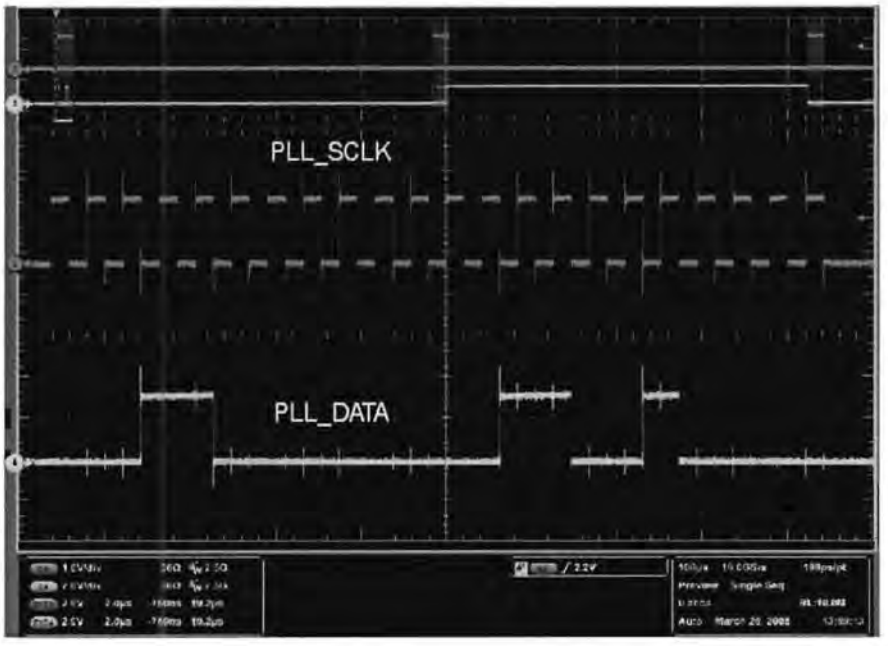


Figure 4.1: 1st 22-bit Word for the *LMX2313U*

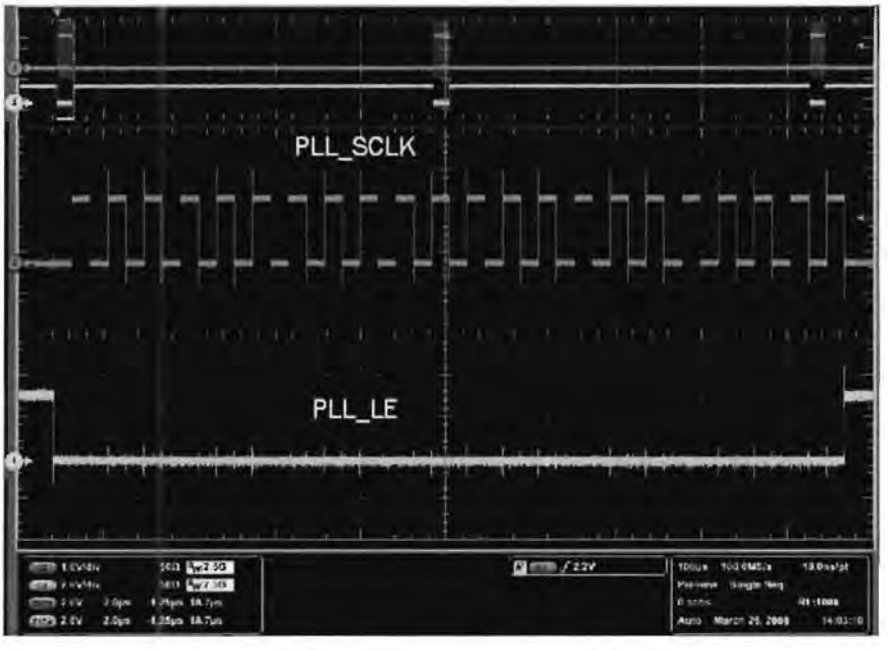


Figure 4.2: 1st Assertion of LE after the Transmission of the 22-bit Word for the *LMX2313U*

Figure 4.3 shows the 1st word (HEX"11FAFF") being transmitted to the ADC. After all of the eight words were successfully transmitted, the calibration process was successfully performed[2].

[2]The *CAL* pin was monitored to seen to be asserted for more than the required 80 clock cycles.

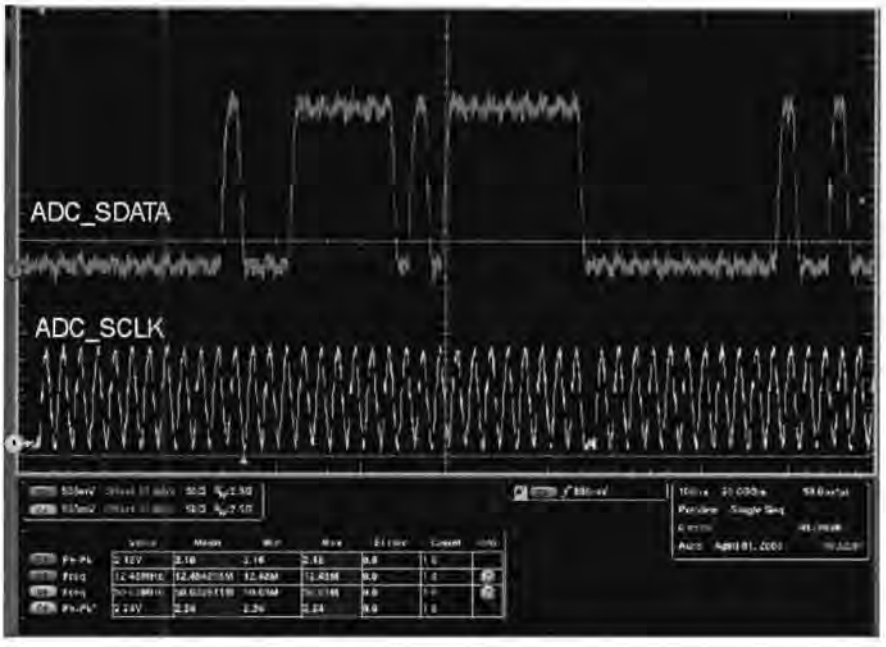


Figure 4.3: 1st 32-bit Word for the *ADC08D500*

4.1.3 PCI-Express Functionality

Although it was originally planned to develop the functionality of the system to a point of allowing data streaming across the PCI-Express interface, time restrictions and design complexity constrained the testing to only assess top-level functionality through the manipulation[3]of the existing *PCI-Express Endpoint IP Core Demo for Lattice ECP2M and SCM* [44].

The card was inserted into suitable PC[4] and the instructions listed in [44] - to get the board 'up and running' - were followed. The accompanying *Microsoft WindowsXP* Java interface read the PCI-Express card information which is shown in *Figure 4.4.*

[3]Altering the 'pin file' to match the designed schematics
[4]One where the motherboard is able to support x4-lane PCI-Express

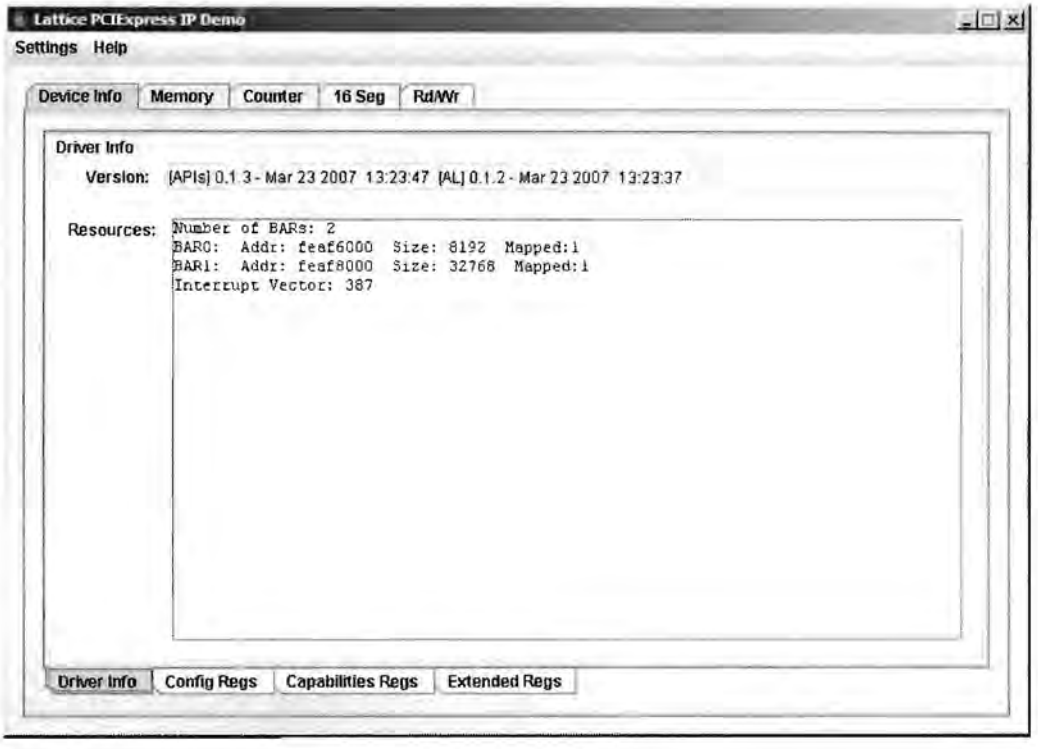


Figure 4.4: PCI-Express Device Information

The demonstration software also allowed the specific tests to be performed on the *AstroGIG* digitizer such as reading/writing from/to the internal FPGA EBR memory (*Figure 4.5*) as well as reading the ECP2M PCI-Express configuration registers (*Figure* 4.6). These same tests were also successfully carried out with a generic PCI driver written under *Ubuntu Linux* (v2.6.24 64-bit).

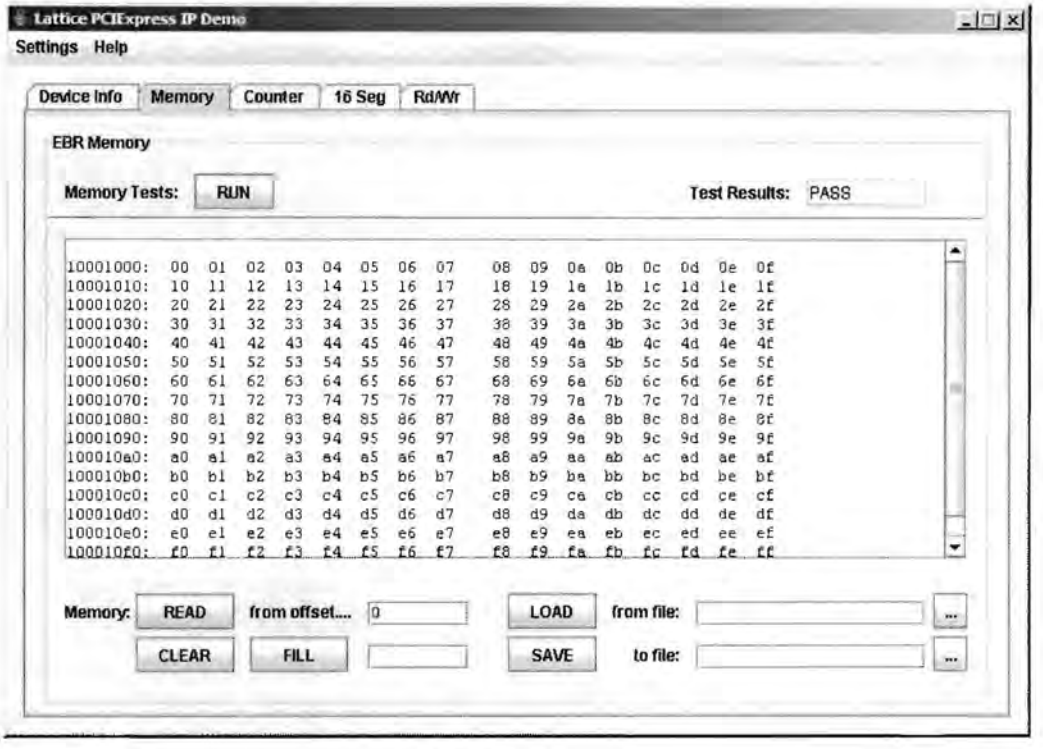


Figure 4.5: EBR Memory Tests

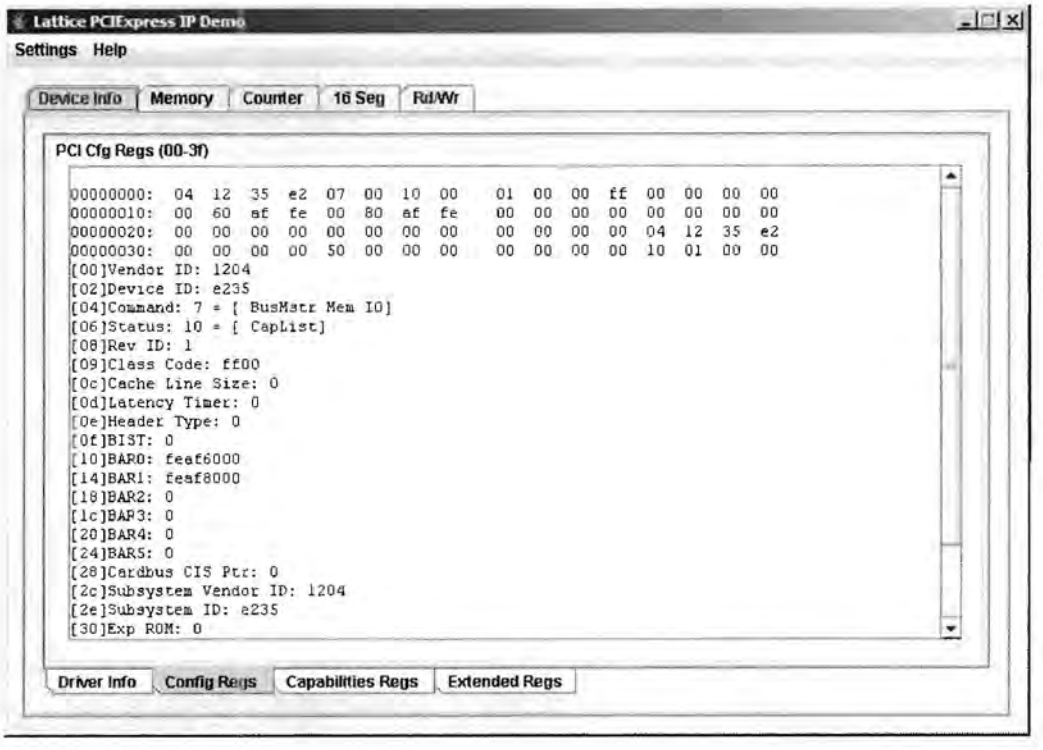


Figure 4.6: Internal PCI-Express Configuration Registers of the *AstroGIG*

These results show that the *AstroGIG* is:

- Fully compliant with the PCI-Express standard.
- Able to send and receive instructions from a host PC.
- Platform independent.
- Capable - with more development - of streaming sampled data through the PCI-Express interface.

4.2 Performance Testing

Using the user specification as an outline, a testing strategy and methodology was developed in order to characterize the performance of the *AstroGIG* sampler. The testing setup overview is illustrated in *Figure 4.7* with the *AstroGIG* powered off a 12V bench Power-Supply-Unit (PSU). Two signal generators provided the necessary sampling clock and signal source to be captured, which were fed into J4 and J2/J1 respectively. The serial and programming cables were attached and the firmware - described in *Section 3.2.2* - was loaded into the FPGA according to the steps given in *Section 3.2.1*.

This testing setup allows a block of data to be captured and transmitted to the PC via the RS232 port. A combination of *WindowsXP HyperTerminal* (to monitor the serial port and write an ASCII *.txt file with the received data) and an ASCII to decimal converter (convert the ASCII *.txt file into a decimal numbers) were used to get the datasets into a format that could be imported into *MATLAB 7.0*. The *MATLAB* code can be found in *Appendix* F.

4.2.1 Analogue Front End

In order to sufficiently characterize the input system, both time and frequency domain responses of the AFE were required.

Various amplitude 100MHz tones were input into the system. The difference between the mathematical ideal[5] and measured values across the AFE input system were observed and are presented in *Table 4.1*. A more conclusive range of input power levels and frequency tones can be found in *Section 4.2.4*.

The s_{11} parameter forms part of the scattering matrix and is a measure of the reflection looking into the *AstroGIG* input ports from what would be the HSHS telescope [24]. The

[5]Calculated by tracing through the power levels as depicted in *Figure 2.4*

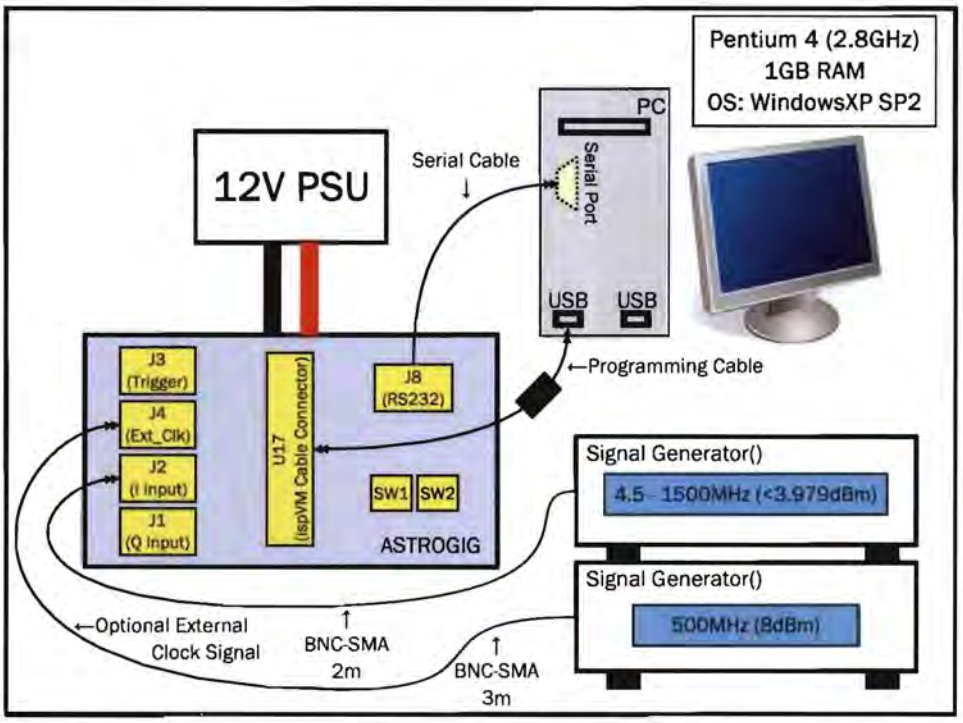


Figure 4.7: Performance Testing Setup Overview

Input 100MHz Tone	*Input at SMA (Vp)*	*Theoretical BALUN Output (Vpp)*	*Measured BALUN Output (Vpp)*
-3dBm	0.2238	0.333	0.3416
0dBm	0.316	0.470	0.4704
3dBm	0.446	0.668	0.6696

Table 4.1: Differences Between the Ideal and Measured BALUN Output

SWR must be known by the antenna designer because the drive amplifier must be modeled as not to create a standing wave and severe reflections between the antenna and digitizer. The s_{11} and hence SWR reflection parameter for both input channels was measured using a vector network analyzer and is shown in *Figures 4.8* and *4.9* respectively.

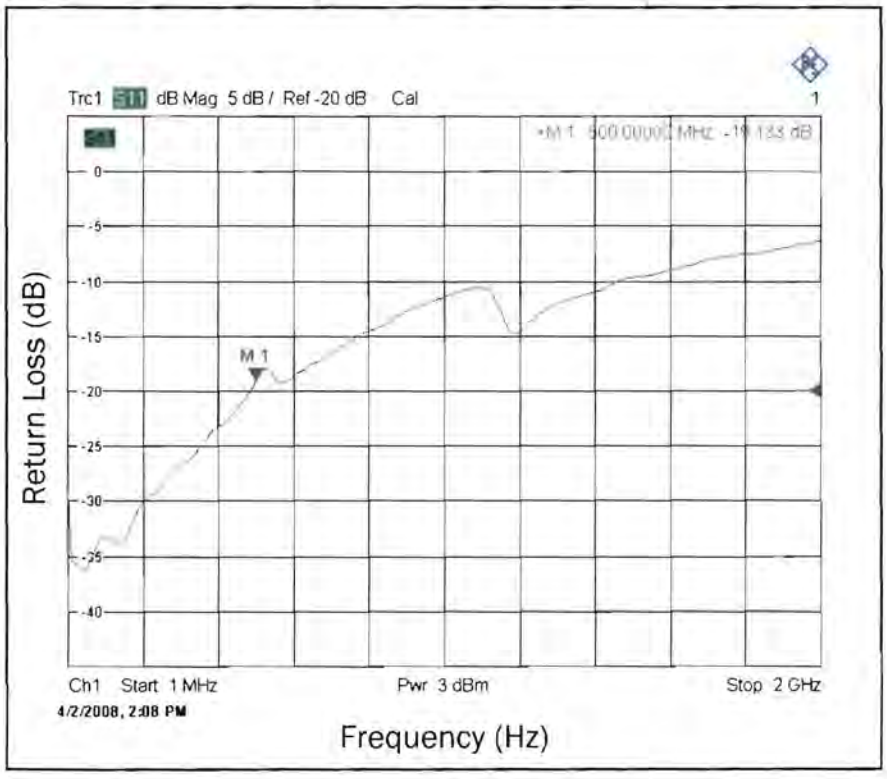


Figure 4.8: Measured SWR in dB for the *AstroGIG* I Input Channel

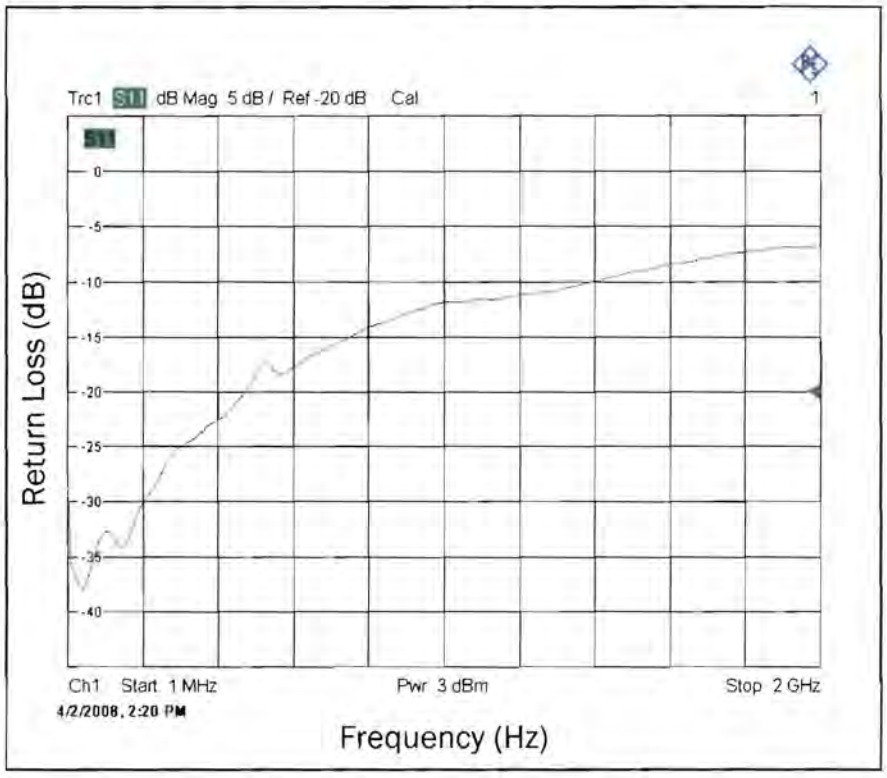


Figure 4.9: Measured SWR in dB for the *AstroGIG* Q Input Channel

4.2.2 On-Board Frequency Synthesizer

The PLL was configured for a VCO output setpoint of 500MHz. The resulting waveforms[6] *(Figures 4.10* and *4.11)* were acquired by probing before the BALUN conversion - on capacitor C49[7] - with an oscilloscope rated for a maximum input frequency of $\leq$ 500MHz[8].

[6]Before BALUN differential conversion
[7]Refer to the schematics of *Appendix F*
[8]500MHz is the 3dB bandwidth

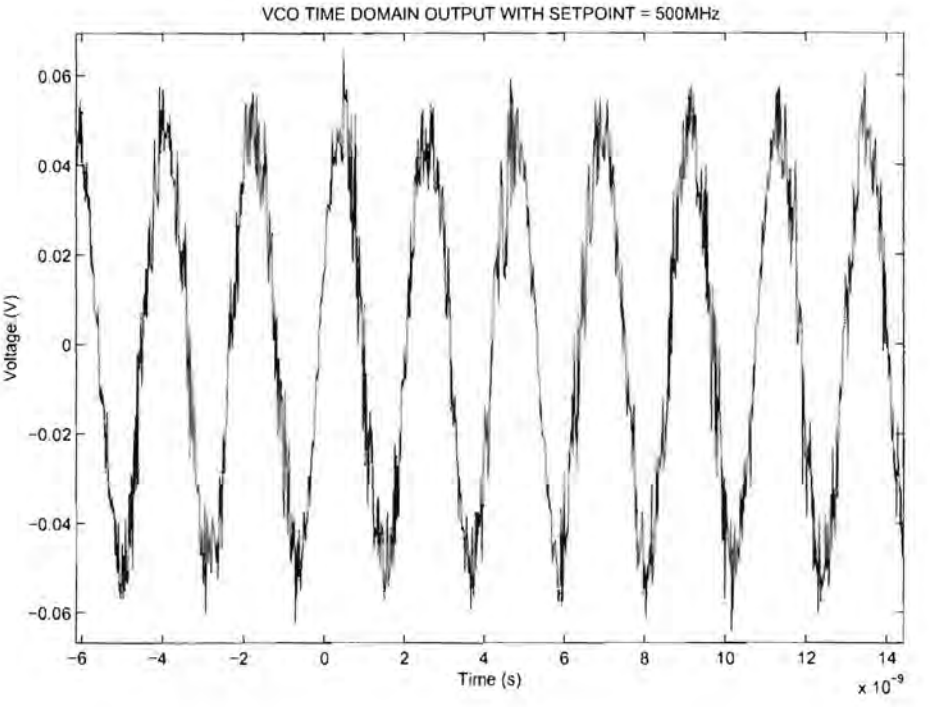


Figure 4.10: Frequency Synthesizer 500MHz Sampling Clock

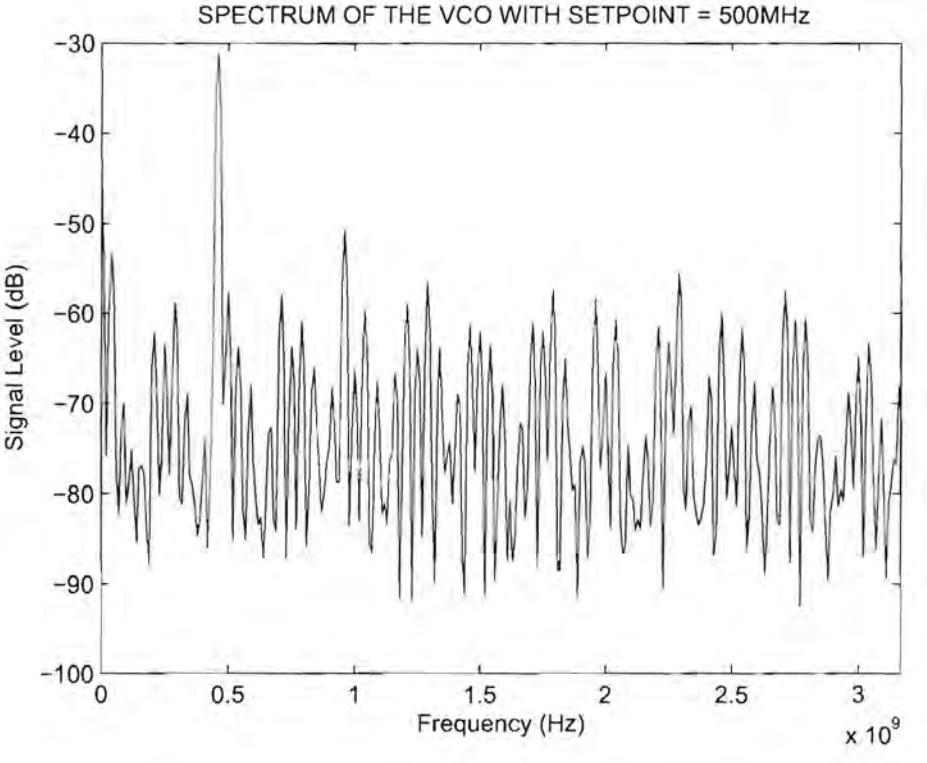


Figure 4.11: Magnitude Spectrum of the 500MHz Sampling Clock

4.2.3 Determining the Noise Floor

This test was conducted by sampling both I and Q channels in a terminated 50Ω impedance, in order to discover if any internal mechanism created spurs in the sampling process. *Figures 4.12* and *4.13* show the noise floor for channel I and Q is ≈-70dB and ≈-60dB respectively.

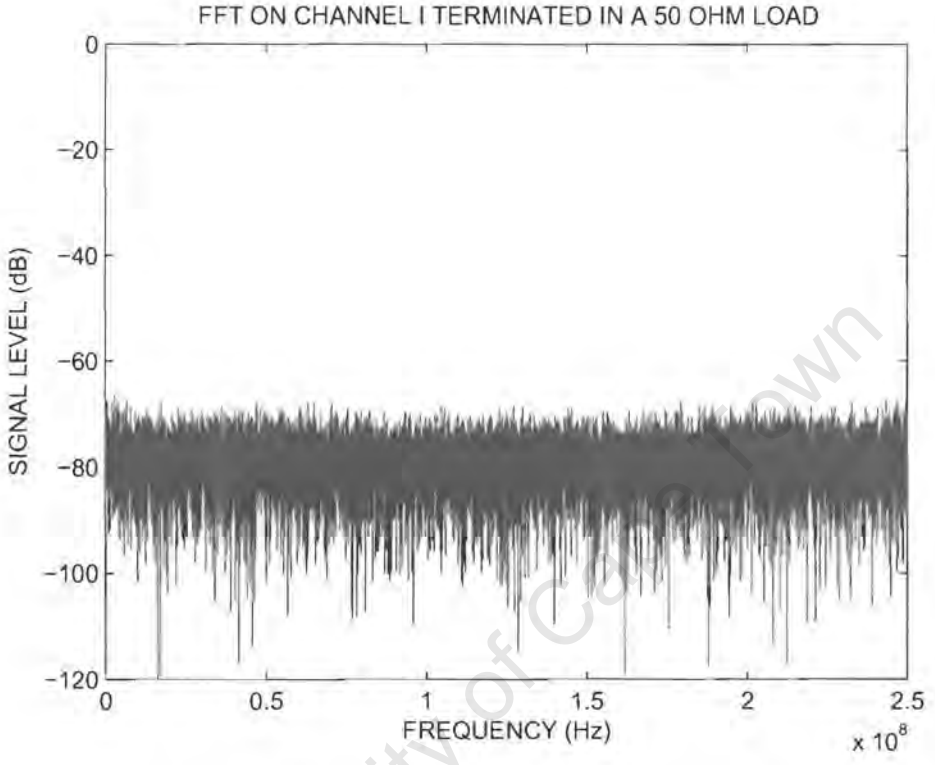


Figure 4.12: Noise Floor of Channel I Terminated in a 50Ω Load

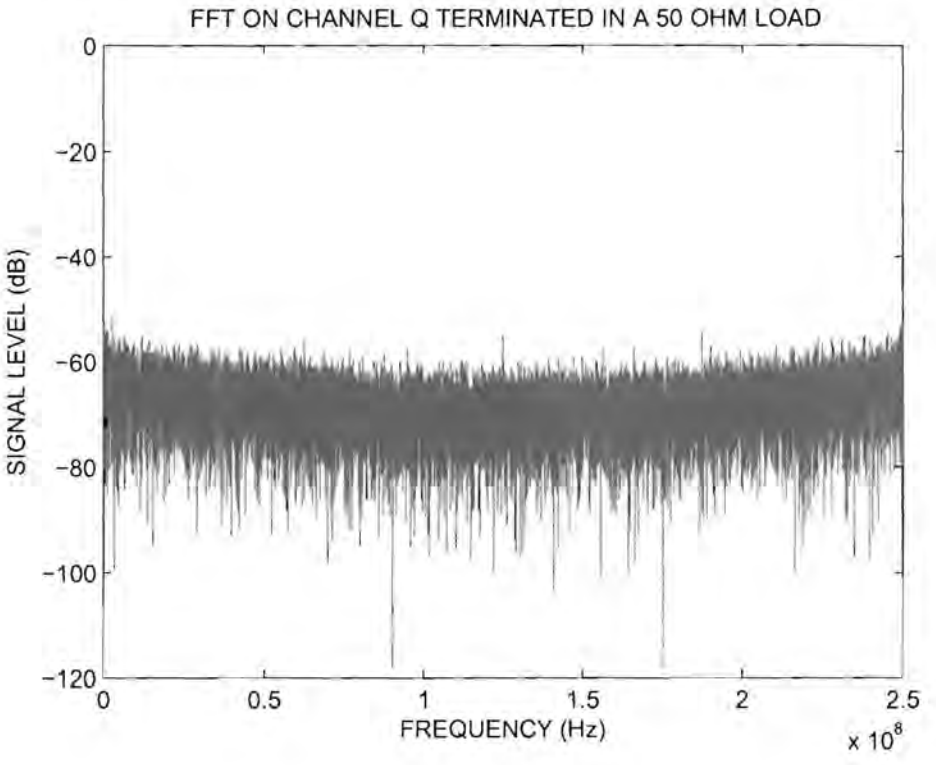


Figure 4.13: Noise Floor of Channel Q Terminated in a 50Ω Load

4.2.4 Capturing Time-Domain Data

Various signals on both input channels where sampled at 500MSPS with 8 bit resolution using an external 500MHz sampling clock at a level of 8dBm into 50Ω. The resulting time domain data sets were examined using *MATLAB 7.0* (*Figures 4.14 - 4.16*):

4.2.4.1 Channel I

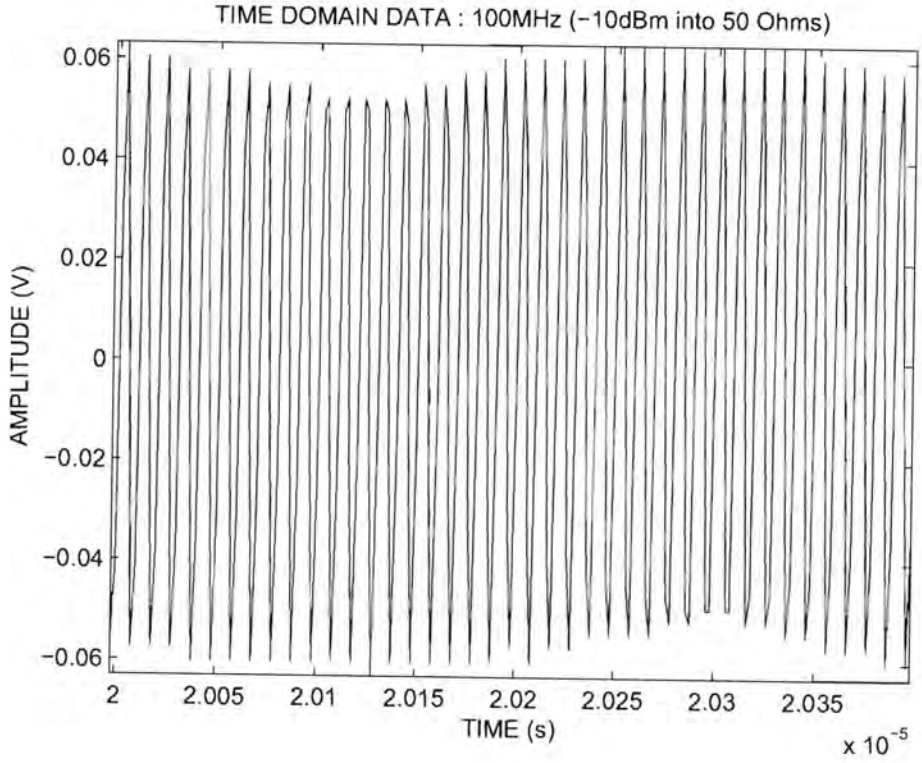


Figure 4.14: Time Domain Capture of a 100MHz Signal at -10dBm

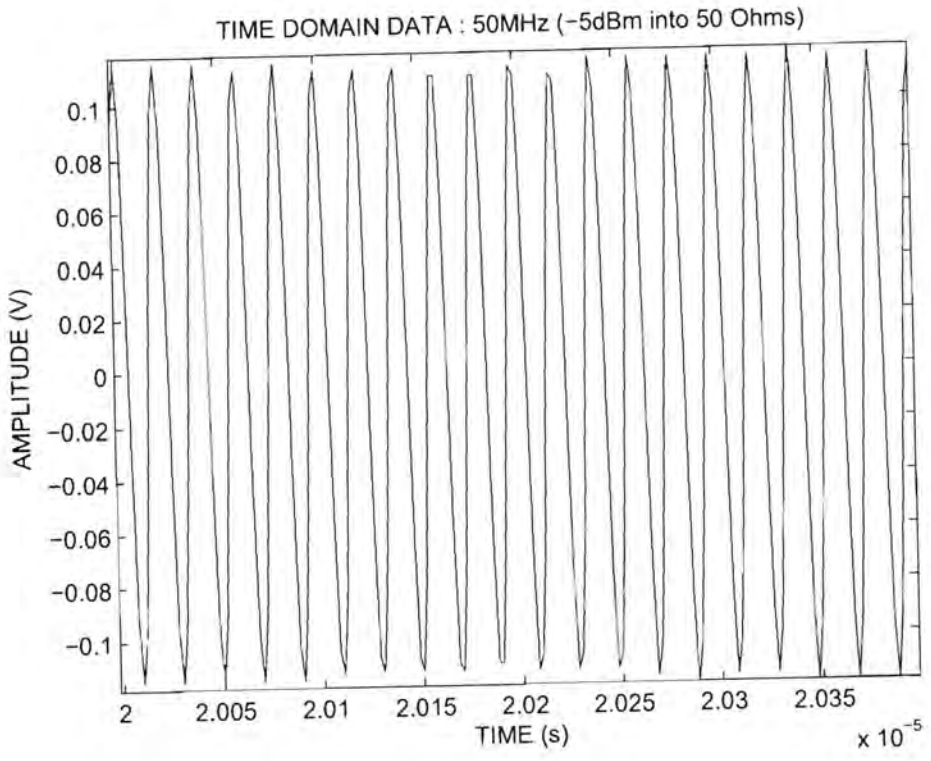


Figure 4.15: Time Domain Capture of a 50MHz Signal at -5dBm

4.2.4.2 Channel Q

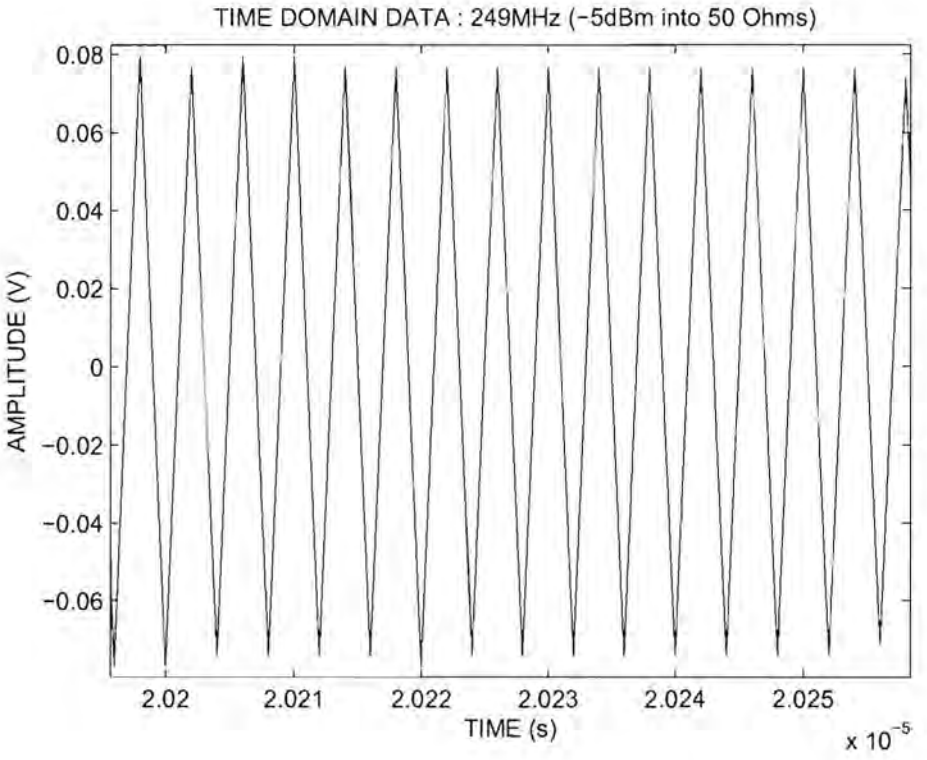


Figure 4.16: Time Domain Capture of a 249MHz Signal at -5dBm

4.2.5 Determining the SFDR and Intermodulation

Once the system had satisfied the functional testing, the analogue performance needed to be determined in terms of SFDR. This was accomplished by examining a selection of captured datasets in the frequency domain (*Figures 4.17 - 4.25*):

4.2.5.1 Channel I

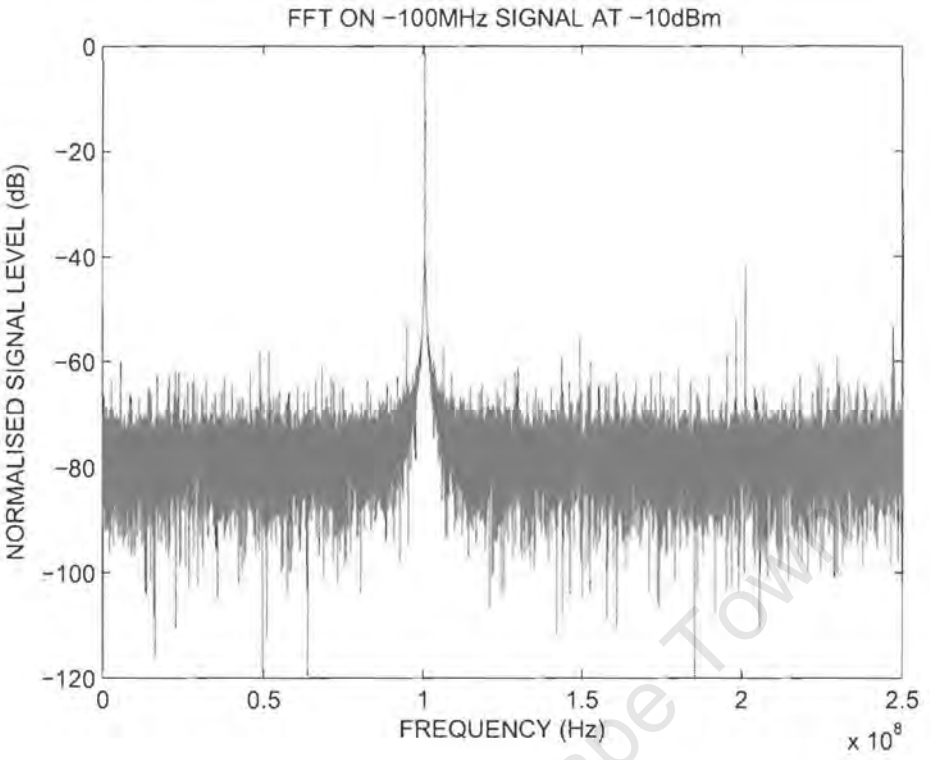


Figure 4.17: FFT of a 100MHz signal at -10dBm

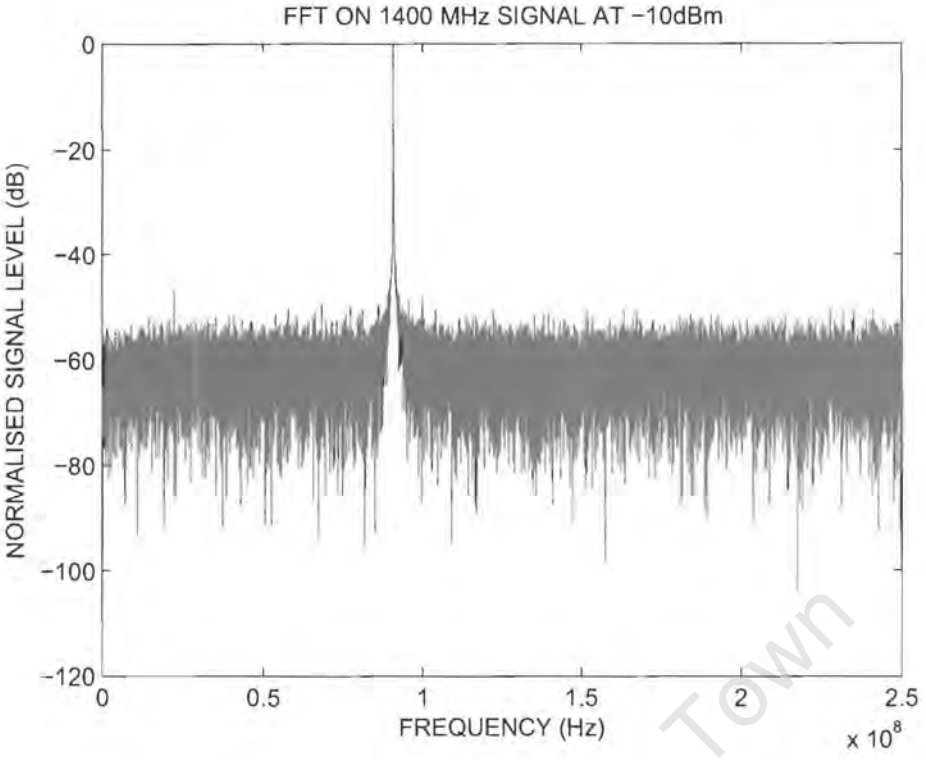


Figure 4.18: FFT of a 1400MHz signal at -10dBm

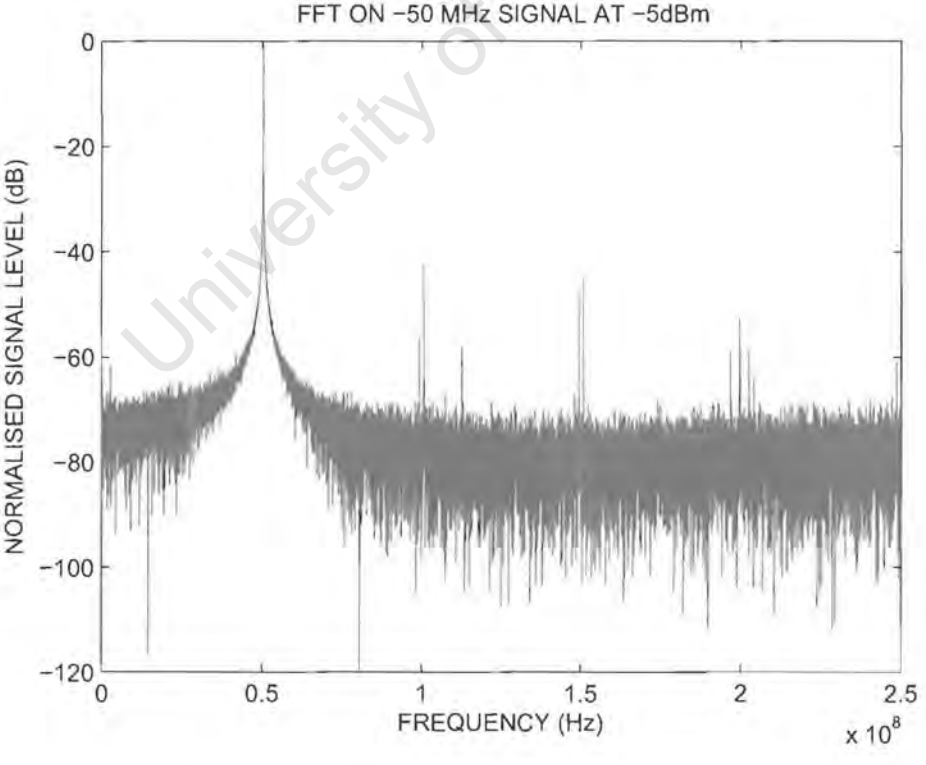


Figure 4.19: FFT of a 50MHz signal at -5dBm

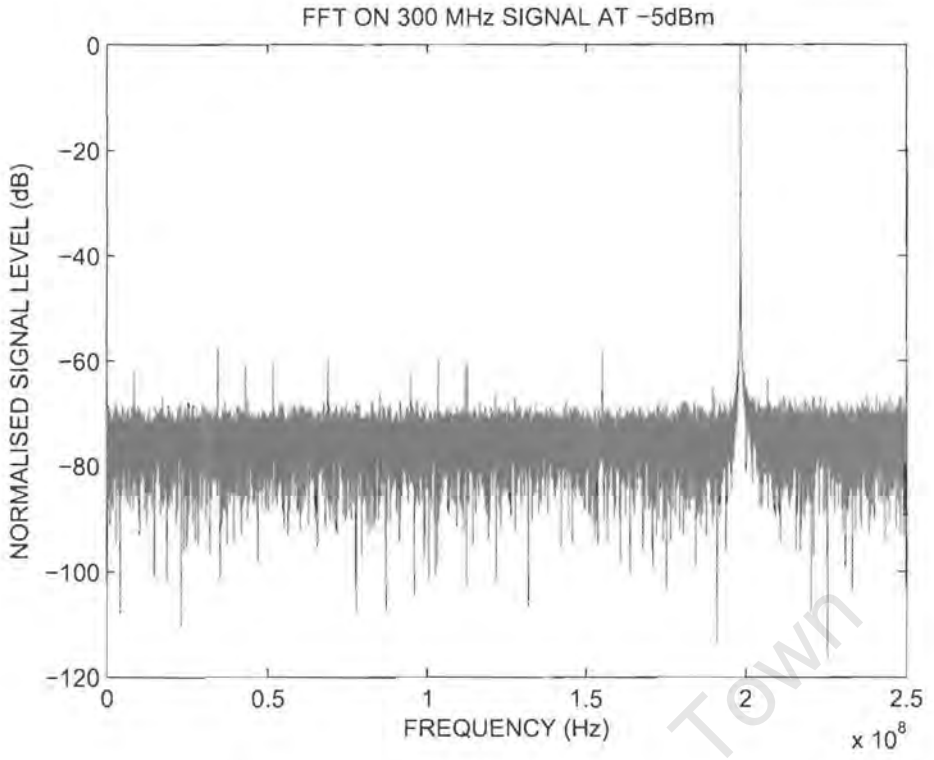


Figure 4.20: FFT of a 300MHz signal at -5dBm

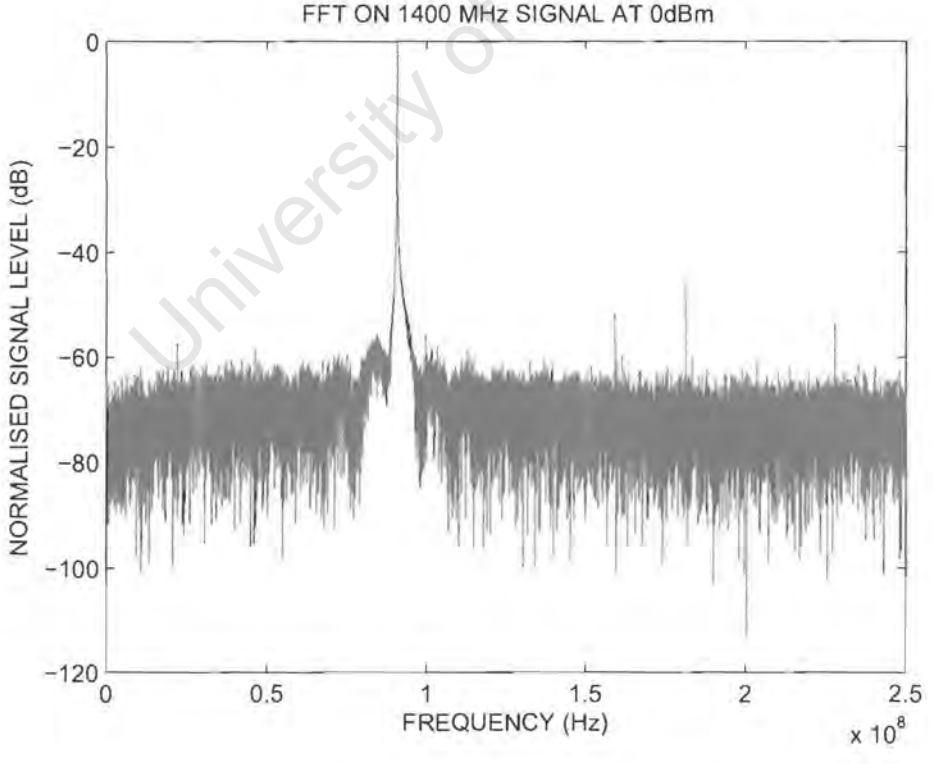


Figure 4.21: FFT of a 1400MHz signal at 0dBm

4.2.5.2 Channel Q

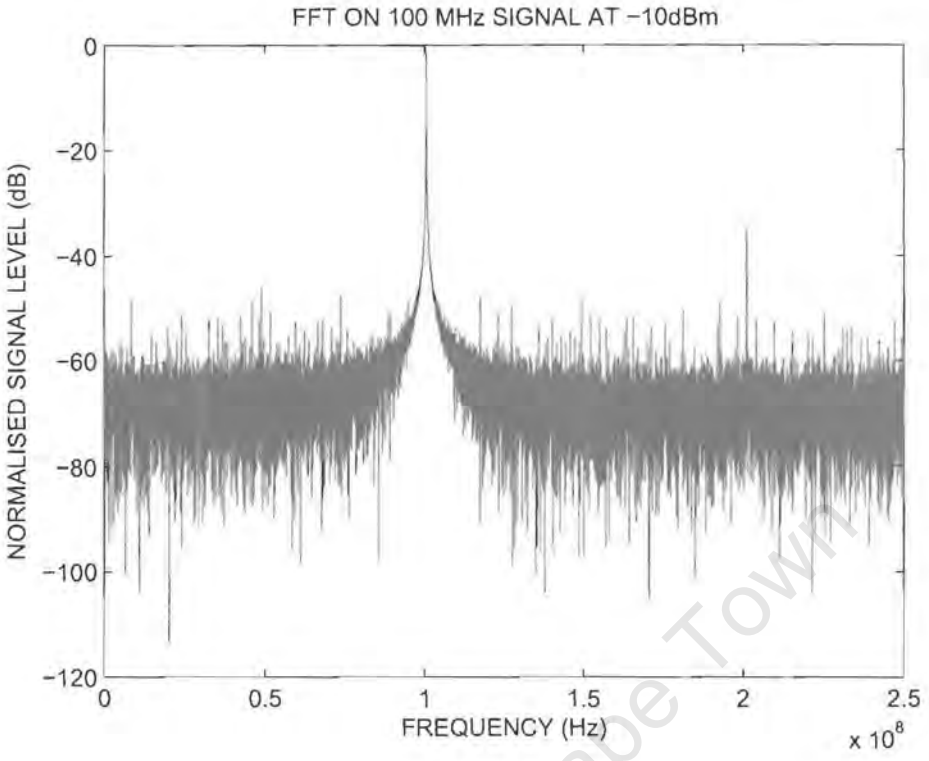


Figure 4.22: FFT of a 100MHz signal at -10dBm

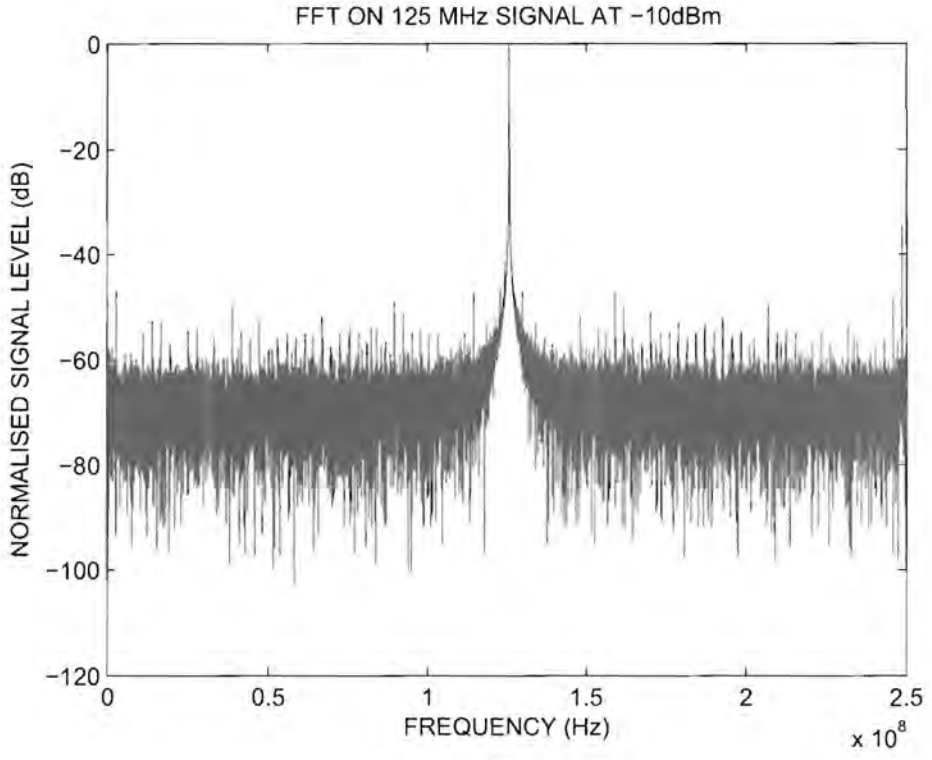


Figure 4.23: FFT of a 125MHz signal at -10dBm

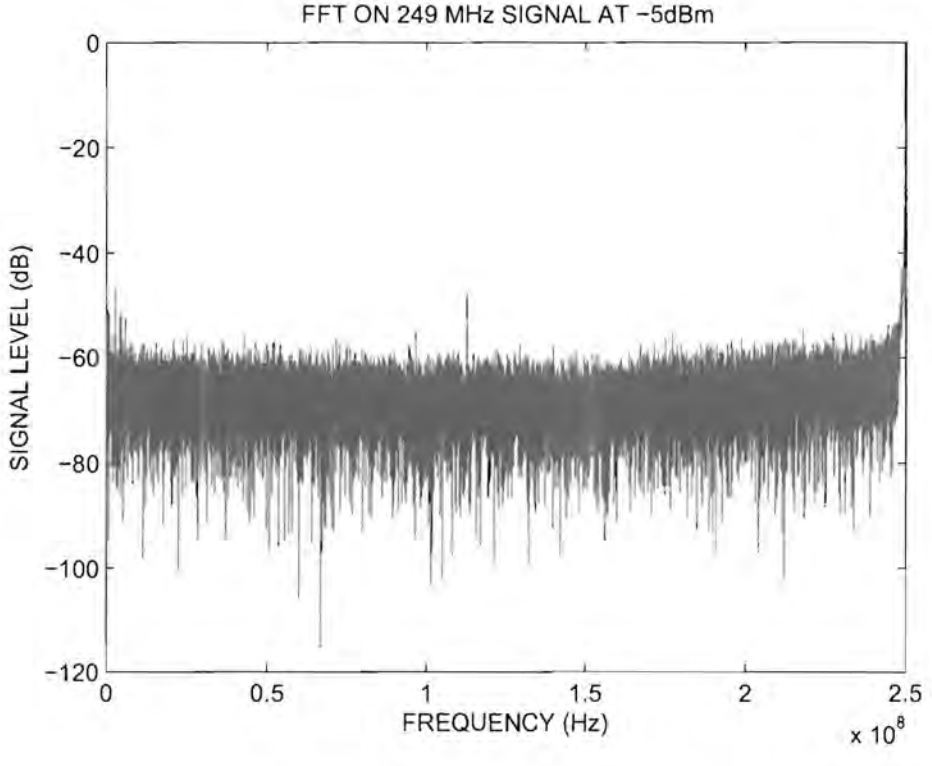


Figure 4.24: FFT of a 249MHz signal at -5dBm

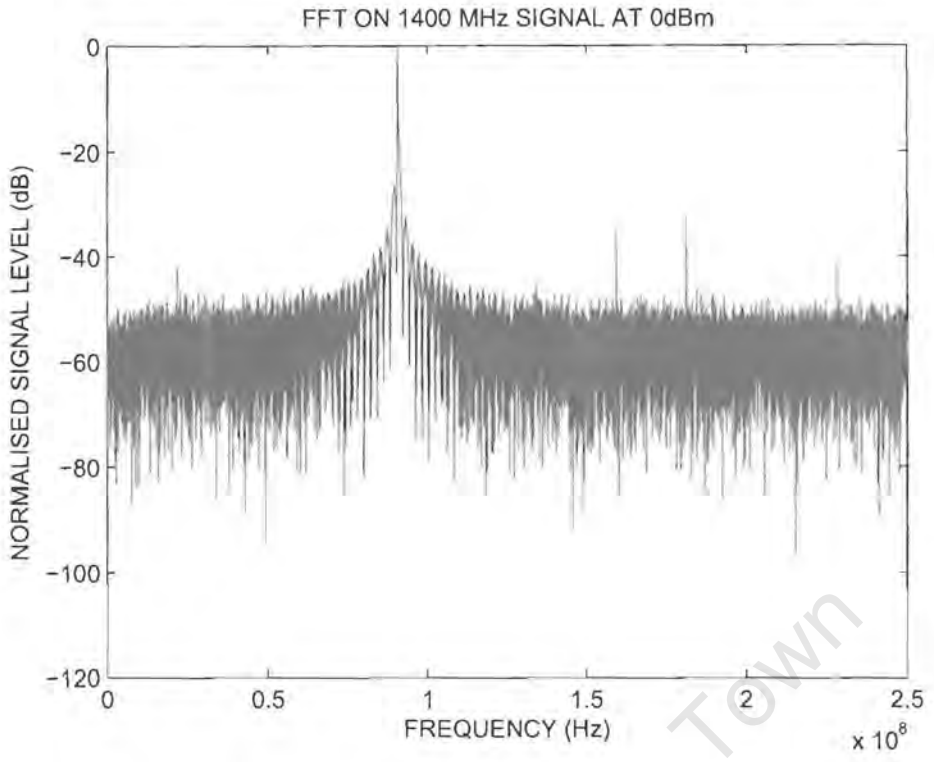


Figure 4.25: FFT of a 1400MHz signal at 0dBm

4.2.5.3 Two-Tone Intermodulation

Figures 4.26 and *4.27* show the frequency spectrum of two tone intermodulation test conducted with inputs at 200MHz and 202MHz respectively.

4.2.5.4 Channel I

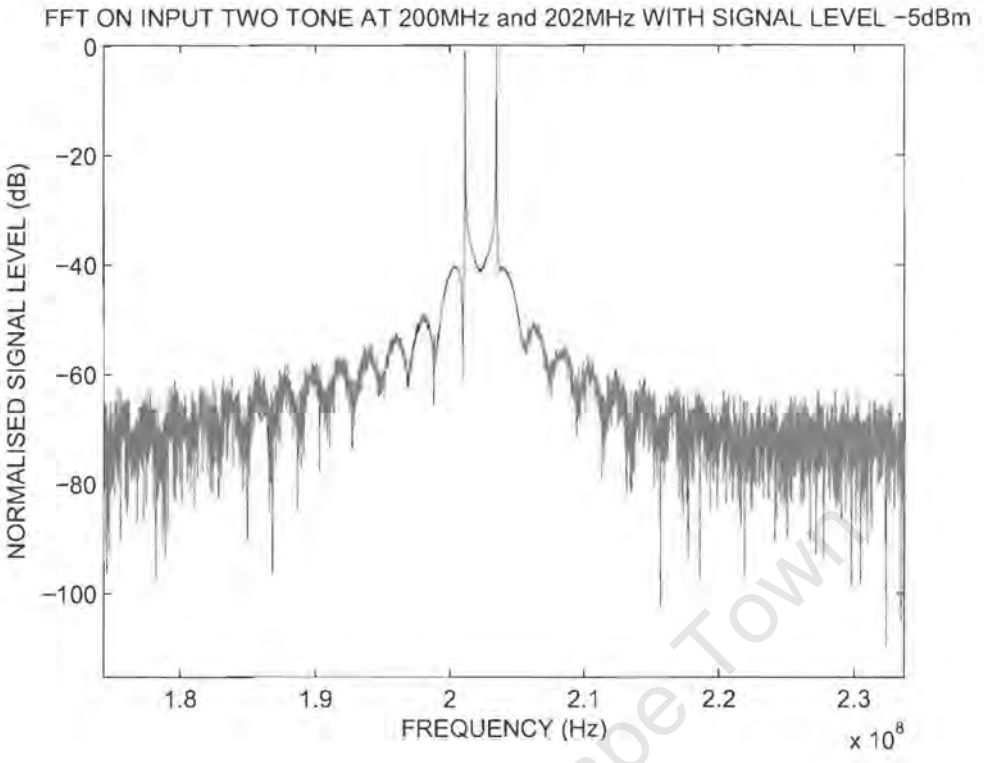


Figure 4.26: FFT of Two Tone Inputs at 200MHz and 202MHz

4.2.5.5 Channel Q

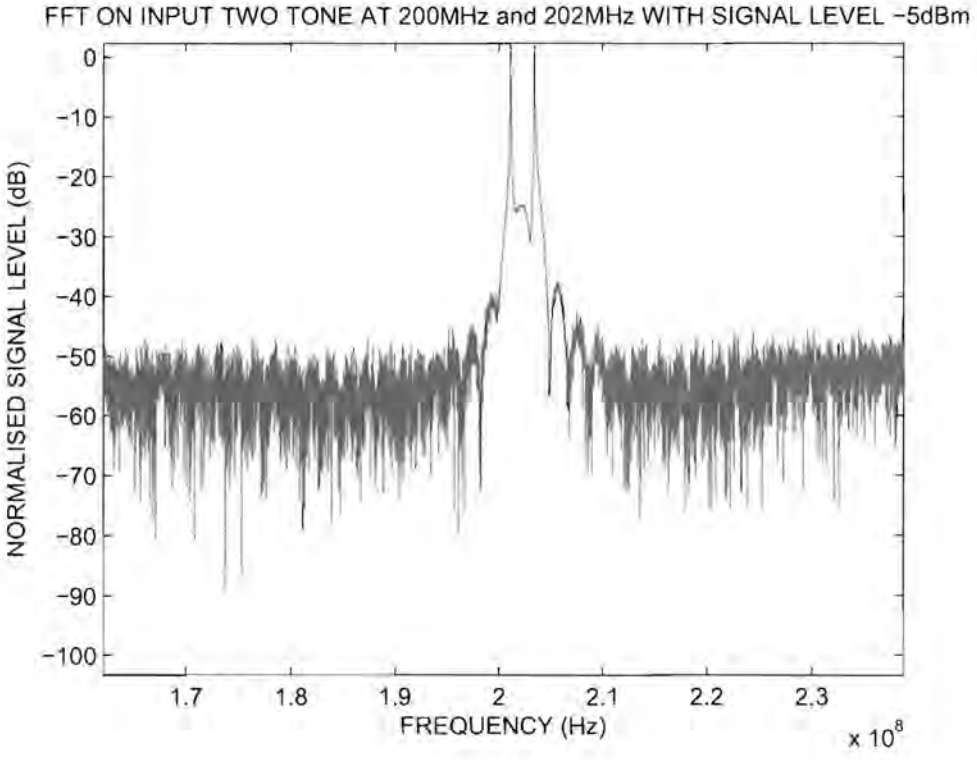


Figure 4.27: FFT of Two Tone Inputs at 200MHz and 202MHz

A discussion of the test results follow in the next Section.

4.3 Analysis of the Performance Testing Results

The on-board frequency synthesizer did not perform as expected. The ADC08D500 sampling clock requires a minimum differential voltage of ≥ 0.4Vpp which equates to ≥ 0.8Vpp before the BALUN differential conversion. *Figure 4.10* showed that the frequency synthesizer only provided ≈ 0.16Vpp and thus was not able to be used as the sampling clock. A $2:1$ BALUN such as the *Minicircuits* ADTL2-18+ used in [28] should rather be implemented in design in order to increase the differential voltage levels to an appropriate value. The other issue was, that although the VCO frequency spectrum peak (*Figure 4.11*) exhibited a SNR of $\approx$ 50dB, it was located at $\approx$ 460MHz with the PLL programmed to have a VCO setpoint of 500MHz. This indicated that the VCO tuning voltage from the loop filter was below the VCO input tuning sensitivity[9]. A SPICE simulation - which can be found in *Appendix D* - was conducted to compare the *AstroGIG* an

[9]Refer to Section 2.3.3

the *National Semiconductor Big Gig Reference Board* loop filter designs with the later providing≈ 30dB more gain than former. Using the values of the *Big Gig* design would put the measured *AstroGIG* loop filter output voltage of ≈ 150mV in the center of the VCO tuning range. Due to these factors jitter measurements could not be taken and be compared to the *WebBench* design[10].

The SWR - for both input channels - was seen to be below 2 : 1 for frequencies $\leq$ 1.5GHz and thus the AFE has an operating efficiency of $\geq$ 66% with only $\leq$ 9.54 dB return loss. The sharp decrease in the SWR (return loss) of channel I at ≈ 1GHz could not be properly explained and requires a thorough investigation. The AFE provided 3.45dB gain throughout the specified frequency range f where 5MHz$\leq f \leq$1500MHz. This is evident from the amplitude of the captured time domain signals of *Section 4.2.4*. These figures also showed that both the signal source and clock generator drifted with time as they were not precise digital instruments.

The noise floor was determined to be ≈-70dB and ≈-60dB for channel I and Q respectively. The discrepancy in the two values was attributed to the drift of the 500MHz external sampling clock. The 'clean' noise spectrum of *Figures 4.12* and *4.13* showed that the there was no significant coupling of leaking clocks into the digitizing system. From the FFT's shown in *Section 4.2.5* it can be seen that the system SFDR was around ≈ 40dBc. This performance level is acceptable for most signal analysis applications including the HSHS. The actual SFDR could be higher as the artifacts in the frequency spectrum are due to the following:

- Coupling of FM bands (88MHz-108MHz) into the ≈3m cables used to feed the signals into the *AstroGIG*[11].
- Harmonics at $mf_1 \pm nf_2$ $m,n\varepsilon\mathbb{Z}$ where f_1 and f_2 are the 500MHz clock signal and signal frequency respectively. A table of these values was calculated up to the 5th-order harmonics[12]. These harmonics were found to alias back into the 1st Nyquist zone and contribute to the spurs seen in *Figures 4.17 - 4.25.*

The two-tone intermodulation tests were conducted with an input power level of -5dBm (50Ω) and frequencies of 200MHz (f_1) and 202MHz (f_2). The third order products should lie at $2f_1 \pm f_2$ and $2f_2 \pm f_1$ or 198MHz and 204MHz respectively [24]. These products could not be seen in *Figures 4.26* and *4.27* because the data - from which these figures were created - needed to be apodized with a Hann filter in order to reduce the ringing. If the input signal power were also increased to maximum the magnitude of the products would also increase significantly.

[10]Refer to *Section 2.3.4*
[11]See *Figure 4.7*
[12]Refer to *Appendix F*

Chapter 5

Conclusions

The aim of this project was to design, develop and implement a high-speed data capture card for the HSHS. The following conclusions as to the success of the project were drawn up:

A hardware platform was developed that conformed to the user requirements for the HSHS. The design and implementation process included:

- Transforming the user specifications into pure electrical engineering terms as well as understanding the principles and concepts involved in mixed signal design (analogue and digital signals).
- Schematic capture, board layout/routing and simulation of the routed PCB with the interpretation of the simulated results in making minor adjustments to the design.
- FPGA firmware development in both VHDL and Verilog.

A low cost design was achieved as the *AstroGIG* is approximately ZAR 8000 cheaper than an OTS unit with similar functionality. Coupled by the *AstroGIG* having four times better theoretical output data rate than these OTS units, it is thus approximately the same order of magnitude more cost effective to implement. It can therefore be seen that the *AstroGIG* is capable of competing with these units in a cost sensitive environment and can therefore reach a broader target market.

The system showed that it was capable of functioning within a multi-platform[1] PCI-Express environment. Although time constraints did not allow data to be streamed through the PCI-Express interface, the *PCI-Express Endpoint IP Core Demo* provided a test-bench on which to base that this capability is possible through further development.

[1] *Linux* and *Microsoft Windows*

The on-board frequency synthesizer did not perform as expected. The reasons for this were that the *AstroGIG* loop filter output voltage was below the input tuning sensitivity of the VCO190-492T[2] and the 1:1 BALUN used to perform the differential conversion only transmitted -3dB power to the ADC clock input. However, this can be corrected by using the same technique as the *National Semiconductor Big Gig Reference Board* by implementing the *Minicircuits* ADTL2-18+ 2:1Ω BALUN. Due to these factors jitter measurements could not be taken and be compared to the *WebBench* design[3].

In terms of analogue performance, the system was found to be adequate for the signal processing applications of the HSHS. The SWR - for both input channels - was seen to be below 2 : 1 for frequencies $\leq$ 1.5GHz and thus the analogue front end has an operating efficiency of $\geq$ 66% with only $\leq$ 9.54 dB return loss. The sharp decrease in the SWR of channel I at $\approx$ 1GHz could not be properly explained. The AFE provided 3.45dB gain throughout the specified frequency range f where 5MHz$\leq f \leq$1500MHz. The noise floor was seen to be at $\approx$-65dB, with an average SFDR of $\approx$40dB for both input channels. No significant coupling of leaking clocks into the digitizing system were found in determining the noise floor. The spurs seen in the frequency domain plots were attributed to the coupling of FM radio signals (88MHz-108MHz) as well as aliased signal harmonics in the 1st Nyquist zone at frequencies $mf_1 \pm nf_2$ $m,n\varepsilon\mathbb{Z}$. Clock/signal sources - used to inject the sampling signals - also drifted in frequency and amplitude which was evident from the time domain plots and thus also contributed to increased spurs. The third order products of *Figures 4.26* and *4.27* could not be seen because the data needed to be apodized with a Hann filter to reduce the ringing as well as increasing the input power levels.

A list of board errata is given in *Appendix E.*

The QDR-II memory remains untested.

[2]Refer to Section 2.3.3
[3]Refer to *Section 2.3.4*

Based on these conclusions, the following suggestions for future work and design improvements are recommended:

Use the x4 lane PCI-Express Interface for data-streaming. To realize the full potential of the *AstroGIG*, firmware must be written to allow captured samples to be streamed across the x4 PCI-Express interface at an *optimized* rate. Further integration into the HSHS would also include a FFT of the sampled data to be preformed on the FPGA in order to to reduce the PCI-Express data bandwidth as well as the required PC computations.

Migrate to a Linux driver. *Linux* provides a robust, modifiable and most importantly an open-source operating system. An open-source driver can thus be development Linux that maps the sampled data to a pre-defined memory space for user operations without the need for proprietary software.

Investigate the decrease in SWR. Investigate whether the sharp decrease in the SWR of channel I at $\approx$ 1GHz has a negative impact on the digitizers analogue performance.

Implement the QDR-II memory. Firmware needs to written in order to implement the QDR-II memory for data storage and buffering.

Incorporate the 'design fixes'. Design improvements - listed in *Appendix E* - should be incorporated in subsequent versions of the *AstroGIG*.

Extend the design for x8 lane PCI-Express. An increased theoretical output data rate up of $\leq$2GB/s would negate the latency issues described in *Section 2.4*. This would require an update of the schematics to include the ECP2M-50 FPGA.

Appendix A

BALUN Simulation *Octave* Code

```
%TC1-1-13M+/ADTL2-18+ balun is a current balun, or choke balun, forcing equal and opposite currents to
flow on the line.  If the line and the terminating load is perfectly symmetrical, the voltage baluns will
force the voltages to be equal and opposite and thus the currents flowing from the balun output terminals
will be equal and opposite and there will be no CM-current on the line.  If, however, the line is not
perfectly symmetrical unequal currents, resulting in CM-currents, will appear leading to line radiation.
(HTTP://WWW.SM.LUTH.SE/~URBAN/MASTER/THEORY/4.HTML)

% Using Lect10.pdf assume Zo = sqrt((L-M)/C) = RLoad for differential impedance characteristic (lossless
line)

% For a matched condition (assumed) the Zin = Zs.  Therefore using a 50 Ohm source we need Zin to equal
50 Ohms.  The formula for Zin is given neatly in M.Pozar.  On the output accoring to many pdf's in Balun
directory, the Zout/Zload/Rload must be equal to r*Zs = r*Zin where r is the impedance ratio from output
secondary to input primary winding.

% Using the ABCD matrix and the relations for the current balun (above) we see 2 relationships:  % If
Iin = I and Vin =V then Vout=Vin.*sqrt(r) and Iin = Iout.*sqrt(r).

% Therefore using the above relations and Zin = Zo.*((Rload.*cosh(Gamma.*l)+Zo.*sinh(Gamma.*l)).//(Zo.*cosh(Gamma.*l)+Rlo
we must make Zo the subject of the formula

%NEED TO GET Zo = 50 OHMS

% only simulte teh ideal case -> the cap sets the cutoff of the 3dB

for r=1:2

r %imp ratio

Rsource = 50 ; % 50 Ohm source (Given)

Zin = Rsource % source must see a match (assumed)

C1 = 0; %0.02e-12; % from adc08d500 datasheet ---->put = 0 for ideal case

F = 1e9; % 1GHz signal

R_Termination = 0:25:300;

ADC_Zin = 100/(1+j.*2.*pi.*F.*C1.*100);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% % Setting the vector of Rload Rload = 1./((1./(ADC_Zin))+(1./R_Termination));

Rload(1) = 1./((1./(ADC_Zin)));

Rload = Rload./r;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
x=0:(10e-9./3000):10e-9;

A = 0.8; % input amplitude sine wave

Vs = A*sin(2.*pi.*F.*x); % input Vs

L_Line = 1e-9; %Line inductance set as a contant

C_Line = 1e-9; %Line capacitance set as a contant

Gamma = j.*2*pi*F*sqrt(L_Line*C_Line);

WaveLength = (1./(F*sqrt(L_Line*C_Line))); % working 1 1GHz

l = WaveLength./10; % typically l < wavelength /10

t=tanh(Gamma.*l); % for lack of a better constant

%make Zo the subject of the equation

Zo_1=(((Zin-Rload)+sqrt((Zin-Rload).^2+(4.*t.*t.*Zin.*Rload)))./(2.*t)); % solution 1

Zo_2=(((Zin-Rload)-sqrt((Zin-Rload).^2+(4.*t.*t.*Zin.*Rload)))./(2.*t)); % solution 2

% Now in order to choose a Zo solution the reflection co-eff must be minimised for between Zo and Rload!)

Relflection_Load= (Rload-Zo_1)./(Rload+Zo_1); % releflection at the load

temp = 5400;

for s = 1:length(Relflection_Load)

if (abs(Relflection_Load(s)) == 0)

temp = s;

else

end

end

fprintf("Characteristic_Sol1 %g\n",Zo_1(temp)); fprintf("Characteristic_Sol2 %g\n",Zo_2(temp)); fprintf("Ideal
Load %g\n",Rload(temp)); fprintf("Termination Used %g\n",R_Termination(temp));

Vout1 = (r).*(((Rload(temp)./2).*(Vs))./(Rload(temp).*cosh(Gamma.*l)+Zo_1(temp).*(sinh(Gamma.*l)))); %diff
Vout 1

Vout2 = (r).*((-1.*(Rload(temp)/2).*(Vs))./(Rload(temp).*cosh(Gamma.*l)+Zo_1(temp).*(sinh(Gamma.*l))));
% diff Vout 2

Vout_Diff_pp= Vout1 - Vout2; % output voltage Vpp

Vpp_out_pp = max(abs(Vout_Diff_pp))./2

Relflection_Zin=(Zo_1(temp)-Zin)./(Zo_1(temp)+Zin) % releflection co-eff

Relflection_Load= (Rload(temp)-Zo_1(temp))./(Rload(temp)+Zo_1(temp)) % releflection at the load

VSWR_Zin= (1+abs(Relflection_Zin))./(1-abs(Relflection_Zin)) %VSWR Gen

%plotting results % hold on;

if r==1

figure;

subplot(2,1,1) plot(Vs) title('INPUT VOLTAGE FROM THE SOURCE Vs'); xlabel('Time [s]') ylabel('Voltage
[V]')
```

```
subplot(2,1,2) plot(abs(Vout_Diff_pp)./2,'r'); title('Vpp FOR POSTIVE DIFFERENTIAL @ THE LOAD'); xlabel('Time
[s]') ylabel('Peak-Peak Voltage [V]')

print('INvsOUTr1.eps','-deps') print('INvsOUTr1.png','-dpng')

else

figure;

subplot(2,1,1) plot(Vs) title('INPUT VOLTAGE FROM THE SOURCE Vs'); xlabel('Time [s]') ylabel('Voltage
[V]')

subplot(2,1,2) plot(abs(Vout_Diff_pp)./2,'r'); title('Vpp FOR POSTIVE DIFFERENTIAL @ THE LOAD'); xlabel('Time
[s]') ylabel('Peak-Peak Voltage [V]')

print('INvsOUTr2.eps','-deps') print('INvsOUTr2.png','-dpng')

end

fprintf("\n\n"); end
```

Appendix B

PowerCalc Estimation Spreadsheet

ispLEVER 7.0 - Power Calculator 7.0

Power Model Information

Power Model Format	2.23
Power Model Values	1.00.00
Power Model Status	preliminary

Design and Device Details

Design Name	ECP2M_Power_Estimate
Family	LatticeECP2M
Device	LFE2M35E
Package	FPBGA672
Part Number	LFE2M35E-7F672C

Environment

Vcc	1.2 V
Vccaux	3.3 V
Vccj	3.3 V
Vccpll	1.2 V
Vccio 3.3	3.3 V
Vccio 2.5	2.5 V
Vccio 1.8	1.8 V
Vccio 1.5	1.5 V
Vccio 1.2	1.2 V
Vccb	1.2 V
Vccxp	1.2 V
Ambient Temperature	40°C
Device Variation	Typical Process

Power Summary

Power Est. Design Vcc	5.4907 W
Power Est. Design Vccaux	0.1649 W
Power Est. Design Vccj	0.0099 W
Power Est. Design Vccpll	0.0703 W
Power Est. Design Vccio 3.3	0.2409 W
Power Est. Design Vccio 2.5	0.0258 W
Power Est. Design Vccio 1.8	0.0523 W
Power Est. Design Vccio 1.5	-0.1878 W
Power Est. Design Vccio 1.2	0.016 W
Power Est. Design Vccb	0.1344 W
Power Est. Design Vccxp	0.3408 W
Total Power Est. Design	6.3582 W

Icc Summary

Icc Est. Design Vcc	4.5756 A
Icc Est. Design Vccaux	0.05 A
Icc Est. Design Vccj	0.0030 A
Icc Est. Design Vccpll	0.0586 A
Icc Est. Design Vccio 3.3	0.073 A
Icc Est. Design Vccio 2.5	0.0103 A
Icc Est. Design Vccio 1.8	0.029 A
Icc Est. Design Vccio 1.5	-0.1252 A
Icc Est. Design Vccio 1.2	0.0133 A
Icc Est. Design Vccb	0.112 A
Icc Est. Design Vccxp	0.284 A
Total Icc Est. Design	5.0836 A

Thermal Summary

Ambient Temperature	40°C
Theta Effective	6.88
Junction Temperature	83.74°C

Maximum Safe Ambient	41.22°C
Logic	
DCLK	Dyn. Pwr 0.0030 W
PCIE	Dyn. Pwr 0.0892 W
QDR_K	Dyn. Pwr 0.0477 W
QDR_CQ	Dyn. Pwr 0.0285 W
OSC_IN1	Dyn. Pwr 0.0 W
OSC_IN2	Dyn. Pwr 0.0 W
OSC_IN3	Dyn. Pwr 0.0 W
OSC_IN4	Dyn. Pwr 0.0 W
PHERIPERAL1	Dyn. Pwr 0.0 W
PHERIPERAL2	Dyn. Pwr 0.0 W
Total Logic Power	0.2966 W
Clocks	
DCLK	Dyn. Pwr 0.5583 W
PCIE	Dyn. Pwr 0.4466 W
QDR_K	Dyn. Pwr 0.8039 W
QDR_CQ	Dyn. Pwr 0.8039 W
OSC_IN1	Dyn. Pwr 0.4466 W
OSC_IN2	Dyn. Pwr 0.4466 W
OSC_IN3	Dyn. Pwr 0.4466 W
OSC_IN4	Dyn. Pwr 0.4466 W
PHERIPERAL1	Dyn. Pwr 0.335 W
PHERIPERAL2	Dyn. Pwr 0.2233 W
Total Clocks Power	4.971 W
I/O	
DCLK	Dyn. Pwr 0.0035 W
QDR_CQ	Dyn. Pwr 0.0021 W
QDR_K	Dyn. Pwr 0.2869 W
PHERIPERAL1	Dyn. Pwr 0.0 W
PHERIPERAL1	Dyn. Pwr 0.197 W
PHERIPERAL2	Dyn. Pwr 0.0156 W
PHERIPERAL2	Dyn. Pwr 2.0E-4 W
OSC_IN1	Dyn. Pwr 0.0104 W
OSC_IN2	Dyn. Pwr 0.035 W
OSC_IN3	Dyn. Pwr 0.0104 W
OSC_IN4	Dyn. Pwr 0.0104 W
Total I/O Power	0.2139 W
EBR	
DP RAM	
DCLK & DCLK	Dyn. Pwr 0.0665 W
Total EBR Power	0.0952 W
DSP	
Total DSP Power	0.0027 W
PLL	
DCLK	Dyn. Pwr 0.0094 W
PCIE	Dyn. Pwr 0.0075 W
QDR_K	Dyn. Pwr 0.0135 W
QDR_CQ	Dyn. Pwr 0.0135 W
OSC_IN1	Dyn. Pwr 0.0075 W
OSC_IN2	Dyn. Pwr 0.0075 W
OSC_IN3	Dyn. Pwr 0.0075 W
OSC_IN4	Dyn. Pwr 0.0075 W
Total PLL Power	0.1435 W
DLL	
Total DLL Power	0.0 W
DQSDLL	
Total DQSDLL Power	0.0 W

SERDES	
PCIe	Dyn. Pwr 0.0 W
Total SERDES Power	0.4789 W
Misc	
Total Misc Power	0.1564 W

Appendix C

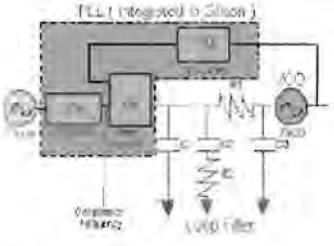
WebBench Specifications

National Semiconductor — WEBENCH®

1 Choose a Part | 2 Create a Design | 3 Analyze a Design | 4 Build It!

Filter Parameters | Components | My Designs

Congratulations on designing your Loop Filter! This section shows your current design which includes your PLL, VCO, and component values for the Loop Filter. You can change your specifications to view new component values, or you can simulate your Loop Filter Design in Analyze a Design. If you wish to use alternative standard components or define custom component values, click on Select Alternative Part.



Your Design #17

Design Name

AstroGIG Frequency Sythesiser

Finished Design

Model	Description	Fmax (Mhz)	Fmin (Mhz)	Price (1k qty)	Options
LMX2313U	Low Power PLL	600	45	$1.26	Samples / Buy Now / Std Eval Board
VCO190-492T	Sirenza VCO	517	466		Alt VCO

Recommended Components — Select All Components or Value

Name	Ideal Value	Std Value	% Diff	Vendor	Part#	Size	Type	Tol
C1	240.0 pF	270.0 pF	12.50 %	Custom	Custom	0603	X7R	10.00 %
C2	6.8 nF	6.8 nF	0.00 %	MuRata	GRM42-6C0G682J50A	1206	C0G/NP0	5.00 %
C3	620.0 pF	560.0 pF	9.68 %	Custom	Custom	0805	NP0	5.00 %
R2	1.6 Kohm	1.6 Kohm	0.00 %	Vishay-Dale	CRCW0805-162JT	0805	0	5.00 %
R3	560.0 Ohm	560.0 Ohm	0.00 %	Vishay-Dale	CRCW0805-561JT	0805	0	5.00 %

Now Analyze a Design

Loop Filter Specification

Comparison Frequency: 1000 KHz help

Output Frequency: 500 MHz help

Part Specific Parameters

				Filter Parameters				Tolerance (help)	Adj Value	% Diff
Charge Pump Gain	4	mA	help	Phase Margin	48	Deg	0%	help	46.5 Deg	3.1 %
VCO Gain	18	MHz/V	help	Loop Bandwidth	10	KHz	Auto	help	33.2 KHz	232.0 %
VCO Input Capacitance	100	pF	help	T3/T1 Ratio	40	%	Auto	help	5.1 %	87.2 %

Update Design

Loop Filter Optimization

Spur Gain Constraints

Spur Offset Frequency: 1000 KHz

Optimization Method (help)

Optimize for: Spur Gain

Locktime Constraints			Optimization Constraints				Achieved Value
Initial Frequency	485	MHz	Max Lock Time	500	uS	help	129.5 uS
Ending Frequency	517	MHz	Max Spur Gain	8	dB	help	2.8 dB
Tolerance	10	Hz	Max High Order Cap	1500	pF	help	620.0 pF

Advanced Settings

Filter Order: 3rd Order help

☐ Allow 2 Parallel Capacitors for Standard Value of C2 help

Resistor Tolerance: 5% help

Capacitor Tolerance: 5% help

Quick Search | Parametric Search | See Our Disclaimer | Product Tree | Back To Webench

Appendix D

SPICE Loop Filter Simulations

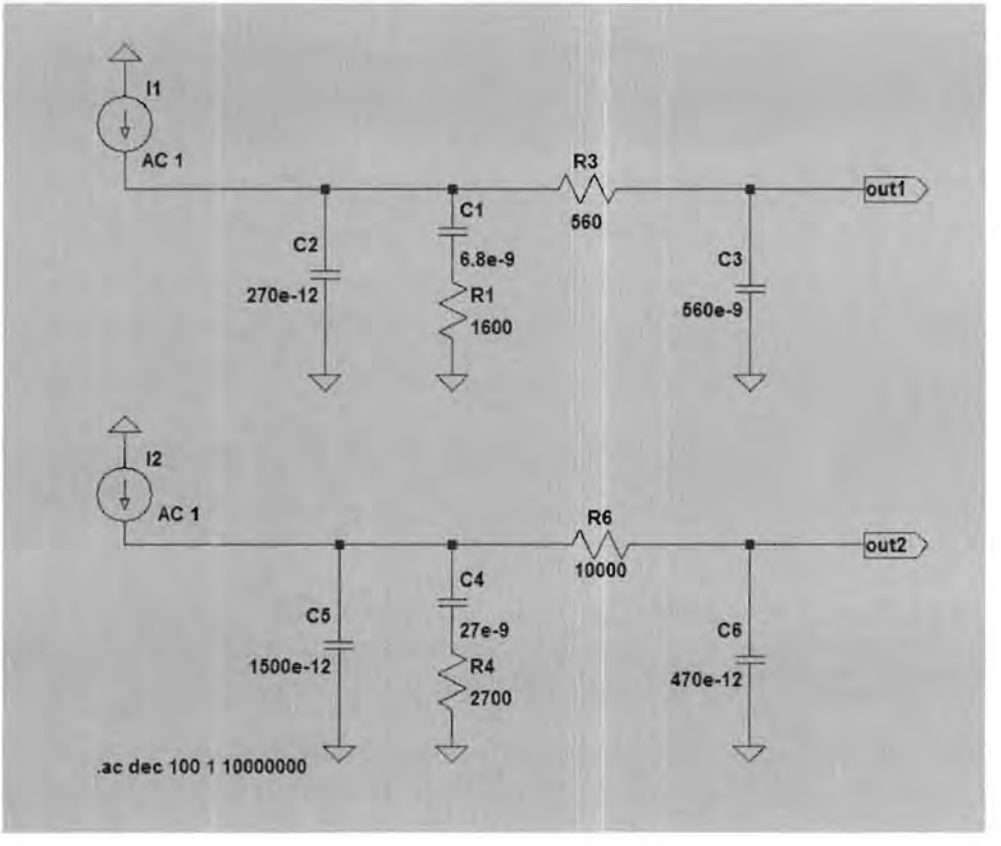


Figure D.1: Loop Filter Curcuit: AstroGIG (Top) vs. BigGIG (Bottom)

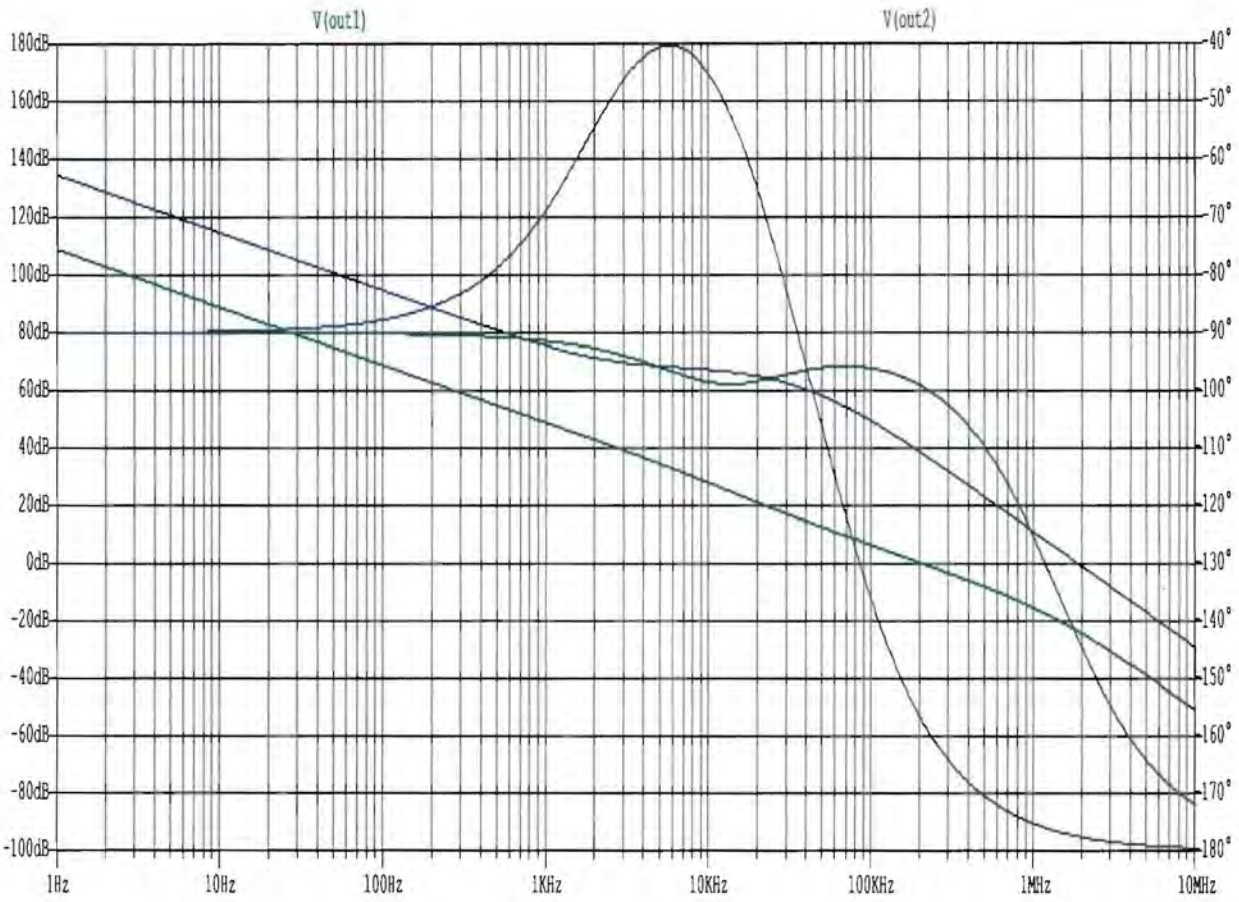


Figure D.2: Loop Filter Responses of the AstroGIG (Green) vs. BigGIG (Blue) Designs

Appendix E

Board Errata

The following design errata should be incorporated into subsequent versions of the *AstroGIG:*

1. Remove Jumper J12 completely from the design.
2. Connect U9.1 to 3V3 through a current limiting resistor ($\approx 18\Omega$).
3. Place testpoints (0Ω resistors) on routes for the 3-wire serial interfaces of the *ADC08D500* and *LMX2313U*. This also allows the 0Ω resistors to be replaced by appropriate current limiting resistors to counteract signal overshoot.
4. Place a testpoint on the FoLD pin of the LMX2313U.
5. Use the values for the *National Semiconductor Big Gig Reference Board* loop filter in order to acheive the correct VCO tuning volatge.
6. Change T3 to the *Minicircuits ADTL2-18+* 1:2Ω Balun so that the differntial output clock meets the minimum ADC input sampling clock requirements.
7. Include a ground header pin in jumper J8.
8. Add extra pushbuttons and LEDs on unused FPGA I/O.
9. Reverse all the silkscreen marking for polarized capacitors because the markings indicate the negative side of the capacitor and not the conventional positive side.
10. Place 100Ω termination resistors at the BALUN transformer outputs.

Appendix F

DVD Attachment

This DVD attachment is included with the disseration and gives all the source code, project files, documentation and simulations not included in the written thesis.

It must be noted that some of the schematic reference designators do not conform with generic names of the IPC standard listed in [69].

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